LV/ULV Mobile Intel® Pentium® III Processor-M and LV/ULV Mobile Intel® Celeron® Processor (0.13 µ) / Intel® 440MX Chipset

Platform Design Guide

April 2002

Order Number: 251012-001

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Rev.	Order Number	Description	Date
001	251012	Initial Release	April 2002

Figure 1. LV/ULV Mobile Pentium III Processor-M / 440MX System Block Diagram

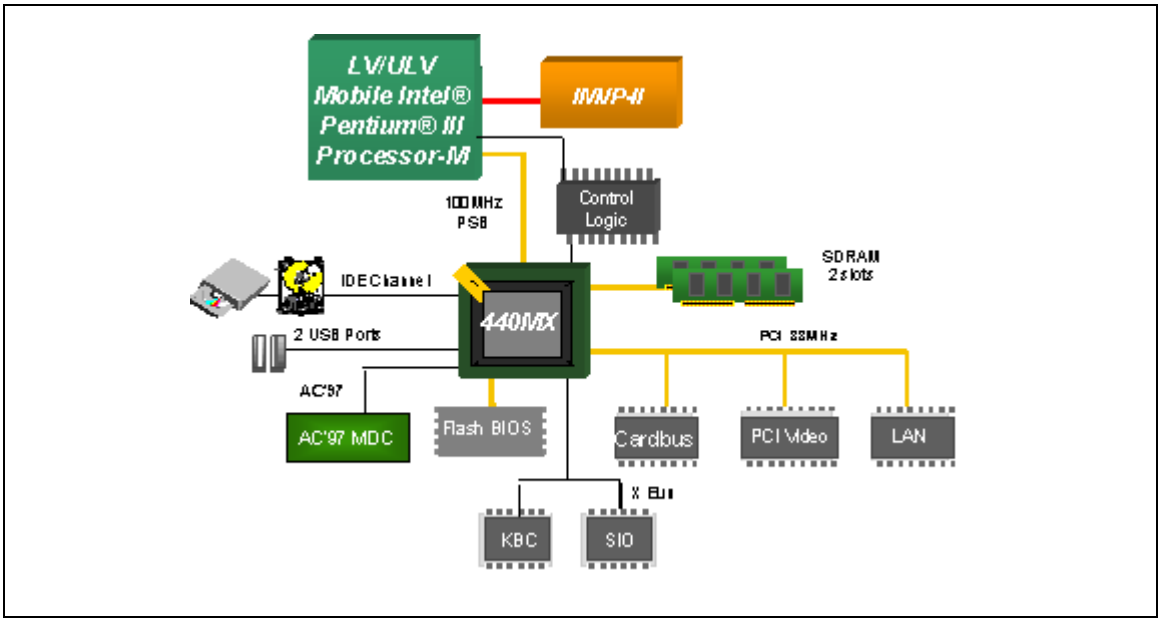
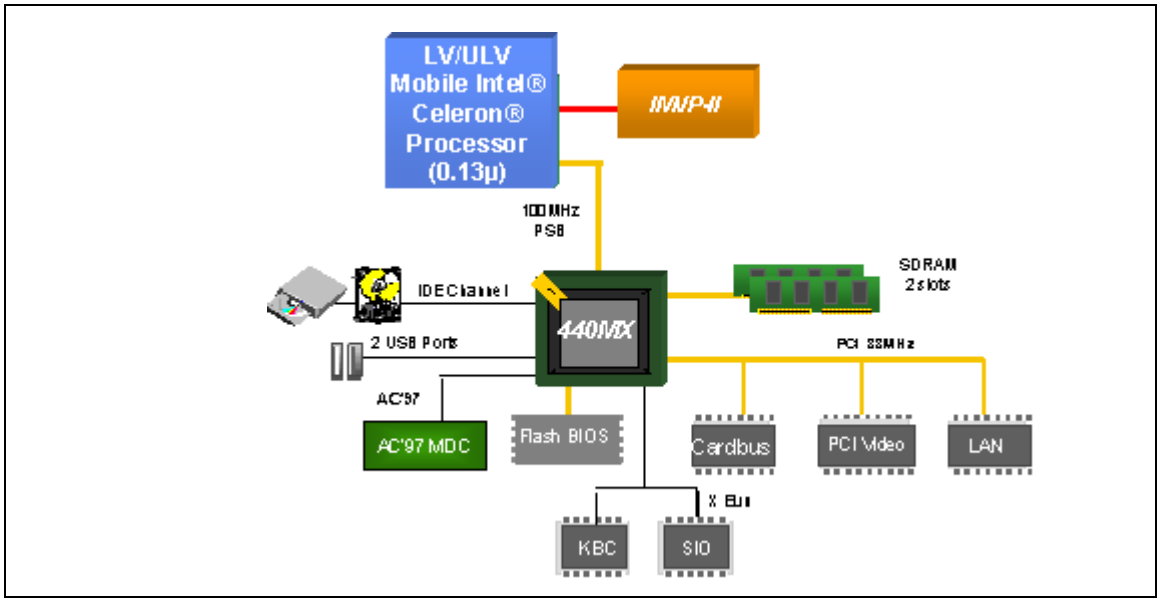


Figure 2. LV/ULV Mobile Celeron Processor (0.13 µ) / 440MX System Block Diagram



1. Introduction

This design guide Intel's design recommendations for Low Voltage / Ultra Low Voltage Mobile Pentium III Processor-M / 440MX systems and includes design recommendations and a system checklist. This document type was formally known as a Recommended Design and Debug Practices (RDDP). These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

1.1. System Overview

Intel offers the 440MX Chipset for the "Mini" and "Sub" notebook segments. The 440MX integrates the two components of Intel's 440BX Chipset – the Intel® 82443BX north bridge and the PIIX4E south bridge. The intent of this document is to provide special design recommendations and concerns to facilitate the development of a system based on the 440MX Chipset and the Low Voltage / Ultra Low Voltage Mobile Pentium III Processor-M (see Figure 1 for a block diagram). To minimize problems during the debug phase, likely design errors have been identified and included in a checklist format in Section 8.

Note that this document describes design and debug practices applicable to a 440MX design operating at a 100-MHz processor system bus and memory interface.

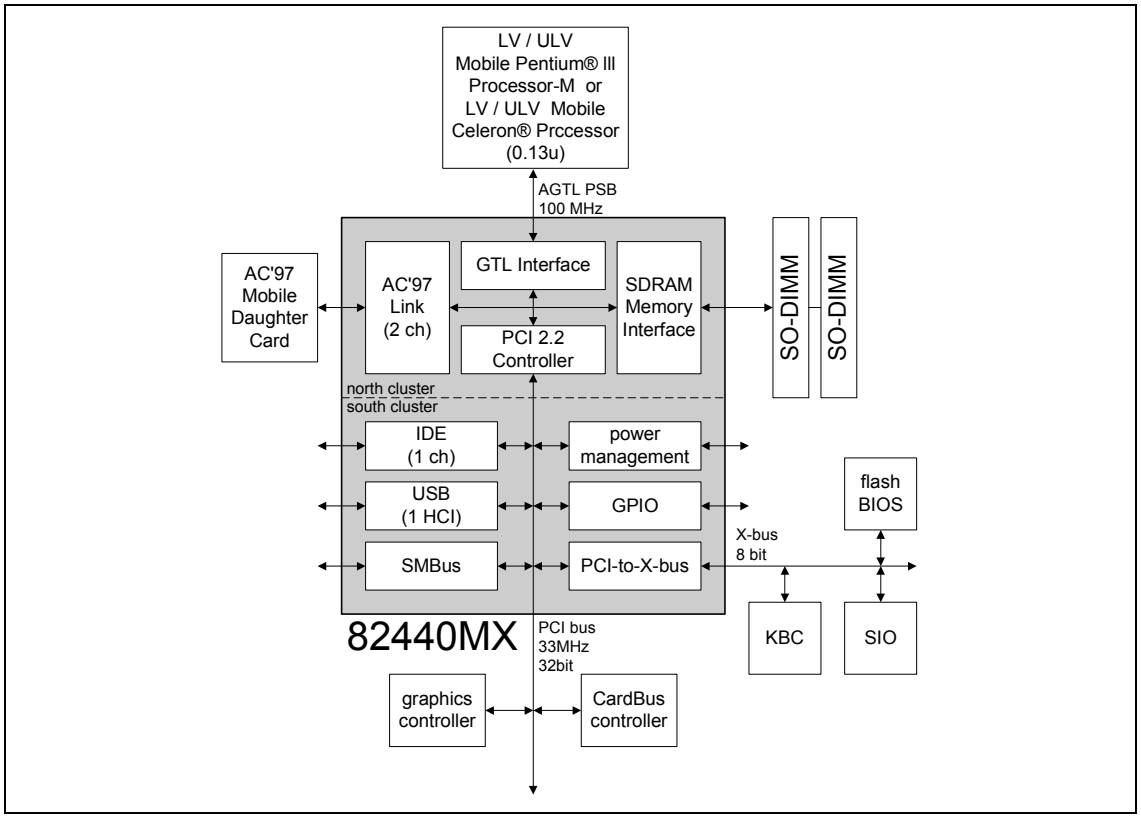
Certain portions of this document have not yet been validated; therefore, if changes to these guidelines are found necessary they will be present in a revision 1.0.

- Full support for Low Voltage (LV) / Ultra Low Voltage (ULV) Mobile Pentium III Processor-M with system bus frequency of 100 MHz (single ended clocking).
  - Featuring Enhanced Intel® SpeedStep® Technology support for multiple processor performance states dynamically
- Full support for Low Voltage (LV) / Ultra Low Voltage (ULV) Mobile Celeron Processor (0.13 µ) with system bus frequency of 100 MHz (single ended clocking).
- 82443MX single-component chipset
- 100-MHz memory interface
  - 64-bit memory data interface (without ECC support)
  - SDRAM support only (no EDO support)
  - Supports a total of 4 rows system memory
  - 16-Mbit, 64-Mbit, and 128-Mbit DRAM technologies supported
- AC'97 host controller
  - Soft modem support*
  - Soft audio support
- PCI rev 2.2 Compliant Bridge
  - Supports 4 PCI masters
  - 4th PCI master is muxed with GPIO signals

* Refer to Section 8.4.1.1 for considerations using AC'97 soft modem and low power platform enhancements.

- Integrated IDE Controller with Ultra DMA/33 support
  - PIO Mode 4 transfers
  - PCI IDE Bus Master support
  - Single channel IDE only
- Integrated Universal Serial Bus (USB) Controller with 2 USB ports
- Integrated system power management support
- PCI-to-X-bus bridge
- System Management Bus (SMBus) Controller
- General purpose inputs and outputs

Figure 3. LV/ ULV Mobile Pentium III Processor-M or LV/ULV Mobile Celeron Processor (0.13µ) / 440MX System Block Diagram



1.2. References

- *Mobile Intel® Pentium® III Processor-M Datasheet* (298340-003): See http://developer.intel.com/design/mobile/datashts/298340.htm
- *Mobile Intel® Celeron® Processor (0.13µ) in Micro-FCBGA and Micro-FCPGA Packages Datasheet* (298517-002): See http://developer.intel.com/design/mobile/datashts/298517.htm
- *PCI Local bus Specification 2.2*: See www.pcisig.com
- *Intel® 82443MX 100 MHz PCISet Datasheet* (245292-001): See http://developer.intel.com/design/chipsets/datashts/245292.htm

- *Intel® 82443MX PCISet Electrical and Thermal Specification Datasheet Addendum (273502-001)*: See http://developer.intel.com/design/chipsets/datashts/273502.htm
- *Intel® 82443MX PCIset Specification Updates (245051-004):* See *http://developer.intel.com/design/chipsets/specupdt/245051.htm*
- *CK97/CK100 Clock Synthesizer / Driver Specification June 1998 (243867-001):* See http://www.intel.com/design/pentiumii/applnots/243867.htm
- *System Management Bus Specification 2.0*. See http://www.smbus.org/specs/
- *Intel® Architecture Software Developer's Manual, Volume 1: Basic Architecture (245470):* See http://www.intel.com/design/pentium4/manuals/245470.htm
- *Intel® Architecture Software Developer's Manual, Volume 2: Instruction Set Reference (245471):* See http://developer.intel.com/design/pentium4/manuals/245471.htm
- *Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide (244472):* See http://developer.intel.com/design/pentium4/manuals/245472.htm
- *Intel® Architecture MMX™ Technology Developer's Guide (243006-001)*
- *AP-524 Pentium® Pro Processor Low Power GTL+ Layout Guidelines (242765-001)*
- *AP-525 Pentium® Pro Processor Thermal Design Guidelines (242766-001)*
- *AP-485* CPUID App note *(Order Number: 241618):* See http://developer.intel.com/design/xeon/applnots/241618.htm
- *AP-585* Layout App note *(Order Number: 243330-001)*
- *AP-586* Thermal App note *(Order Number: 243331-001)*
- *AP-587* Power App note *(Order Number: 243332-001)*
- *AP-589* EMI *(Order Number: 243334-001)*
- *PC100 SDRAM Specification 1.0:* See http://developer.intel.com/technology/memory/UNB_001.htm
- *PC100 SDRAM Serial Presence Detect (SPD) Specification:* See http://developer.intel.com/technology/memory/
- *PC100 SO-DIMM Specification 1.0:* See http://developer.intel.com/technology/memory/sodm1_0.htm
- *Universal Serial Bus Specification, 1.1*. See*:* http://www.usb.org/developers/docs.html
- *Intel® SpeedStep® Technology Applet* (Contact your field sales representative to obtain applet)
- *Intel® SpeedStep® Technology Applet Install Guide* (Contact your field sales representative to obtain guide)
- *Advanced Configuration and Power Interface (ACPI) Specification 2.0*. See*:* *http://www.teleport.com/~acpi/*

2. Design Guide Introduction

This design guide organizes Intel's design recommendations for LV/ULV Mobile Pentium III Processor-M / 440MX Chipset based systems. The document provides design and debug recommendations and a system checklist. Intel developed these design guidelines to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Consult the debug recommendations when debugging an LV/ULV Mobile Pentium III Processor-M / 440MX Chipset based system. Preview these debug recommendations before completing board design to ensure correct implementation of the debug port and other debug features.

3. Design Features

3.1. Processor

The 440MX Chipset supports LV/ULV Mobile Pentium III Processor-M and LV/ULV Mobile Celeron processor operating at 100-MHz bus frequency. LV/ULV Mobile Pentium III Processor-M integrates processor core and 512 kB of second-level cache memory using 0.13-micron process. LV/ULV Mobile Celeron Processor integrates processor core and 256 kB of second-level cache memory using 0.13-micron process. The Low Voltage (LV) /Ultra Low Voltage (ULV) Mobile Pentium III Processor-M and Mobile Celeron Processor (0.13 µ) use single ended clocking running at 100 MHz. Theses processors also feature a 64-bit wide Low Power AGTL processor system bus (PSB) in a Micro-FCBGA package.

All references to the Mobile Pentium III Processor-M in this document refer to both the Low Voltage and Ultra Low Voltage Mobile Pentium III Processor-M.

All references to the Mobile Celeron processor (0.13 µ) in this document refer to both the Low Voltage and Ultra Low Voltage Mobile Celeron processor.

3.1.1. Enhanced Intel® SpeedStep® Technology

Enhanced Intel SpeedStep technology enables real-time dynamic switching of the voltage and frequency between two performance modes (maximum and battery optimized) based on processor demand. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. On LV/ULV Mobile Pentium III Processor-M based systems, installation of *Intel® SpeedStep® Technology Applet 2.x* or equivalent software is recommended to support Enhanced Intel SpeedStep technology.

Contact your Intel field representative for more information on implementing Intel SpeedStep Technology using Mobile Pentium III Processor-M with 440MX Chipset.

3.1.2. Deeper Sleep

Deeper Sleep is a new dynamic power management mode feature of Mobile Pentium III Processor-M to deliver longer battery life. It reduces a processor voltage below the minimum operating voltage during ACPI C3 while preserving the processor state. Deeper Sleep is functionally identical to the Deep Sleep State but at a 66% lower voltage.

Contact your Intel field representative for more information on implementing Deeper Sleep using Mobile Pentium III Processor-M with 440MX Chipset.

3.2. 440MX Chipset

The 440MX Chipset is a single-component chipset based on the Intel 82440BX Chipset. Refer to Figure 1 and Figure 3 in Section 1.1 for a block diagram of a typical platform based on the 440MX Chipset with LV / ULV Mobile Pentium III Processor-M.

The "north cluster" of the 440MX Chipset component is designed with a Low Power AGTL Processor System Bus to interface with the processor operating at 100 MHz. The "north cluster", in addition to the processor system bus, also includes a PCI revision 2.2-compliant Host-to-PCI bridge interface, is optimized for high-speed memory operation with a 100-MHz, 3.3-V SDRAM memory controller and data path, and integrates an AC'97 host controller.

The "south cluster" of the 440MX component integrates a PCI-to-X-bus bridge function, a high-performance bus-master capable PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function including chip select controls and general purpose input and output pins.

The 440MX Chipset component includes the following functions and capabilities:

- 64-bit Low Power AGTL based system data bus interface
- 32-bit system address bus support
- 64-bit SDRAM main memory interface
- 32-bit PCI bus interface with integrated PCI arbiter
- PCI Rev 2.2 compliant PCI host controller
- PCI-to-X-bus bridge with support for 33-MHz PCI operations
- ACPI power management support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller supporting a single Ultra DMA/33 IDE channel
- USB host interface with support for 2 USB ports
- AC'97 2-codec host interface
- System Management Bus (SMBus) host controller, supports DRAM SO-DIMM serial presence detect
- General purpose input and outputs

3.2.1. Processor System Bus Interface

The 440MX supports a maximum 32-bit (4 Gbytes) system address space and provides a four-deep in-order queue (i.e., it provides pipelining support for up to four outstanding transaction requests on the system bus). The Mobile Pentium III Processor-M and Mobile Celeron Processor includes an integrated L2 cache; all cache control logic is provided on the processor.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded to the PCI bus, depending on the PCI address space being accessed. When accessing a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When accessing a PCI I/O or a memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space.

3.2.2. DRAM Interface

The 440MX integrates a main memory controller that supports a 100 MHz, 64-bit synchronous DRAM interface. The integrated DRAM controller drives a total of four rows of memory (two double-sided SO-

DIMMs) and supports 16-Mbit, 64-Mbit, and 128-Mbit DRAM technology, and provides up to 256 Mbytes of total system memory.

3.2.3. PCI Interface

The 33-MHz PCI interface is Revision 2.2 compliant and supports up to four external PCI bus masters in addition to the internal south cluster functions, which are logically present on the PCI bus at IDSEL 18 (device 07).

3.2.4. System Clocking

The 440MX operates the processor system bus and the memory interface at 100 MHz, and the PCI interface at 33 MHz. The 440MX clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. For details, refer to the CK97/CK100 *Clock Synthesizer / Driver Specification – June 1998* (See Section 1.2 for references).

3.2.5. PCI-to-X-Bus

The 440MX provides a PCI-to-X-bus bridge, integrating many common I/O functions found in ISA-based PC systems, including a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and a Real Time Clock. In addition to compatible transfers, each DMA channel also supports Type F transfers. The 440MX fully supports both PC/PCI and Distributed DMA protocols implementing PCI-based DMA. The interrupt controller has edge- or level-sensitive programmable inputs. Chip select decoding is provided for the BIOS, a keyboard controller, a second external micro-controller, and two programmable address ranges for additional devices. The 440MX provides full Plug-and-Play compatibility. The 440MX can be configured as a Subtractive Decode bridge or as a Positive Decode bridge.

3.2.6. USB Controller

The 440MX contains a Universal Serial Bus (USB) host controller that is Universal Host Controller Interface (UHCI) compatible. The host controller's root hub has two programmable USB ports.

3.2.7. IDE Controller

The 440MX supports a single IDE channel for one or two IDE devices providing an interface for IDE/EIDE hard disks and CD ROMs. 440MX provides support for "Ultra DMA/33" synchronous DMA-compatible devices.

3.2.8. AC'97 Controller

The 440MX integrates an AC'97.2 codec interface, supporting modem* codecs and audio codecs. The AC'97 interface is logically located within the north cluster of the 440MX Chipset to maximize performance and minimize latency.

* Refer to Section 8.4.1.1 for considerations using AC'97 soft modem and low power platform enhancements.

3.2.9. Power Management

The 440MX supports enhanced power management, including full clock control, device management to monitor device activity states, and Suspend and Resume logic with Power-On-Suspend, Suspend-to-RAM or Suspend-to-Disk. It fully supports operating system-directed power management via the Advanced Configuration and Power Interface (ACPI) specification. The 440MX includes a System Management Bus (SMBus) Host and Slave interface for serial communication with other devices.

4. Layout/Routing Guidelines

Warning: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that designers simulate critical signals to ensure proper signal integrity and flight time.

4.1. General Recommendations

The trace impedance typically noted (i.e. 55 Ω ± 15%) is the "nominal" trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces minimizes this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

The following factors impact coupling between two traces: prepreg thickness, coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section, Section 5. Processor System Bus Design Guidelines, Section 6. System Memory Design Guidelines, Section 7. Clocking Guidelines, and Section 8. Design Review Checklists.

Intel created these routing guidelines using the *stack-up* described in Section 4.2. Simulate any circuits that deviate from the recommendations in this design guide.

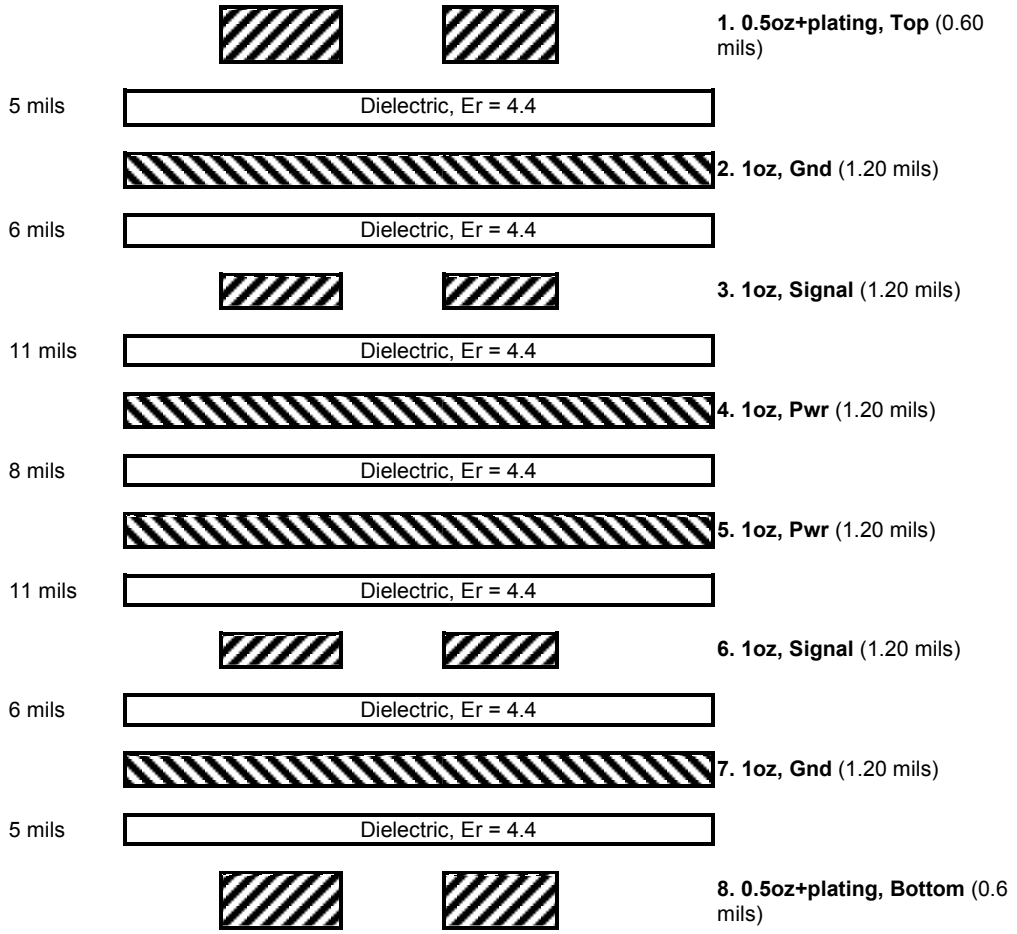
4.2. Nominal Board Stackup

4.2.1. Board Impedance/Stackup Summary

- This is a compilation of the layout guidelines for the Vicuña board. These are recommended guidelines only.
- Via size: 14 drill, 26 pad.

4.2.1.1. Board Stack-Up

There are 8 layers: 4 routing layers, 2 power layers, and 2 ground layers. An example stack-up is shown below.



4.2.1.2. Trace Width and Spacing

All traces should target 55 Ω ±10% unless otherwise specified. Use the following values when routing:

	55 Ω single ended	90 Ω differential	100 Ω differential
	trace / space	trace / space	trace / space
Layers 1 & 8	5.5 / 5.5 mils	6.0 / 6.0 mils	5.0 / 7.0 mils
Layers 3 & 6	5.0 / 5.0 mils	5.5 / 4.5 mils	5.0 / 7.0 mils

4.2.2. Impedance Calculation Tools

3D Field Solvers, such as those by HP*, Ansoft*, Sonnet*, and Polar* provide the most accurate method for calculating impedance. Z calculators based on equations (zcalc) are also fairly accurate

5. Processor System Bus Design Guidelines

5.1. Introduction

LV/ULV Mobile Pentium III Processor-M delivers high performance by integrating the level 2 cache into the processor and running it at the core speed. In addition, these processors will run at a higher core speed than previous generation IA-32 processors. The LV/ULV Mobile Pentium III Processor-M continues to be hardware and software compatible with the current Intel Pentium III processors. Its package type is Micro-Flip Chip Ball Grid Array (Micro-FCBGA).

The following layout guidelines support designs using LV/ULV Mobile Pentium III Processor-M and the 440MX Chipset. Due to on-die Rtt resistors on the processor, additional resistors do not need to be placed on the motherboard for most Processor Side Bus (PSB) signals. The lone exception is on the CPURST# signal which requires a 56-Ω pullup to Vcct on the processor end of the transmission line.

5.1.1. Terminology

For this document, the following terminology applies:

Mobile Pentium III Processor-M refers to Intel's next generation Intel Pentium III processor based on cutting edge 0.13-micron (130 nanometer) technology.

5.2. Processor System Bus (PSB) Routing Guidelines

5.2.1. Timing Analysis

The following table lists the AGTL component timings of Mobile Pentium III Processor-M, Mobile Celeron Processor (0.13 µ) and 440MX Chipset defined at the pins. These timings are for reference only. Refer to processor specifications from the latest datasheet and specification updates. For 440MX Chipset, refer to *Intel® 440MX PCISet Electrical and Thermal Specification Datasheet Addendum*.

Table 1. Processor and Chipset AGTL Parameters for Example Calculations

IC Parameters	Pentium III Processor-M / Celeron Processor (0.13µ) 100-MHz System Bus	440MX	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns	4.45 ns	1
Clock to Output minimum (T_{CO_MIN})	0.40 ns	1.20 ns	1
Setup time (T_{SU_MIN})	1.30 ns	3.00 ns	1,2
Hold time (T_{HOLD})	1.00 ns	-0.10 ns	

NOTES:
1. Check the appropriate component documentation for the latest timing parameter values.
2. T_{SU_MIN} = 3.00 ns assumes that the 440MX Chipset sees a minimum edge rate equal to 0.3 V/ns.

The following table gives an example of AGTL initial maximum flight time and Table 3 is an example minimum flight time calculation for a 100-MHz, uniprocessor system using a Mobile Pentium III Processor-M/ 440MX Chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design**. Table 2 and Table 3 are derived assuming:

- CLK_{SKEW} = 0.15 ns
- CLK_{JITTER} = 0.25 ns
- T_{P-P} = 0.15

See the respective processor's datasheet, appropriate 440MX Chipset documentation, and *CK97/CK100 Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

Table 2. Example TFLT_MAX Calculations for 100-MHz Bus

Driver	Receiver	Clk Period[1]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	440MX	10 ns	3.25 ns	3.00 ns	0.15 ns	0.20 ns	0.20 ns	3.05 ns
440MX	Processor	10 ns	4.45 ns	0.95 ns	0.15 ns	0.20 ns	0.20 ns	3.90 ns

NOTE: $T_{FLT\_MAX} = T_{CYC} - T_{CO\_MAX} - T_{SU\_MIN} - Clk_{SKEW} - Clk_{JITTER} - T_{P-P} - M_{ADJ}$

Table 3. Example TFLT_MIN Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	M_{ADJ}	Recommended T_{FLT_MIN}
Processor	440MX	-0.10 ns	0.15 ns	0.40 ns	0.10 ns	-0.25 ns
440MX	Processor	1.00 ns	0.15 ns	1.20 ns	0.10 ns	-0.25 ns

NOTE: $T_{FLT\_MIN} = T_{HOLD} - T_{CO\_MIN} + T_{P-P} + M_{ADJ}$

The flight times in the previous tables include margin to account for the phenomena listed below that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
- Crosstalk on the PCB and internal to the package can cause variation in the signals.

There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:

- The effective board propagation constant (S_{EFF}), which is a function of:
  - Dielectric constant (ε_r) of the PCB material.
  - The type of traces connecting the components (stripline or microstrip).

— The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

5.3. General Topology and Layout Guidelines

Table 4. Processor System Bus Data Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width & spacing (mils)
CPU	440MX		Max (inches)	Min (inches)		
D[63:0]#	HD[63:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

Table 5. Processor System Bus Address Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width & spacing (mils)
CPU	440MX		Max (inches)	Min (inches)		
A[31:3]#	HA[31:3]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

Table 6. Processor System Bus Control Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width & spacing (mils)
CPU	440MX		Max (inches)	Min (inches)		
RESET#	CPURST#	TOP 2	4.0	2.0	55 ± 15%	5 & 10
BNR#	BNR#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
REQ[4:0]#	HREQ[4:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
BPRI#	BPRI#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DEFER#	DEFER#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
LOCK#	HLOCK#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
TRDY#	HTRDY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DRDY#	DRDY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
ADS#	ADS#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
DBSY#	DBSY#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
HIT#	HIT#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
HITM#	HITM#	TOP 1	4.0	2.0	55 ± 15%	5 & 10
RS[2:0]#	RS[2:0]#	TOP 1	4.0	2.0	55 ± 15%	5 & 10

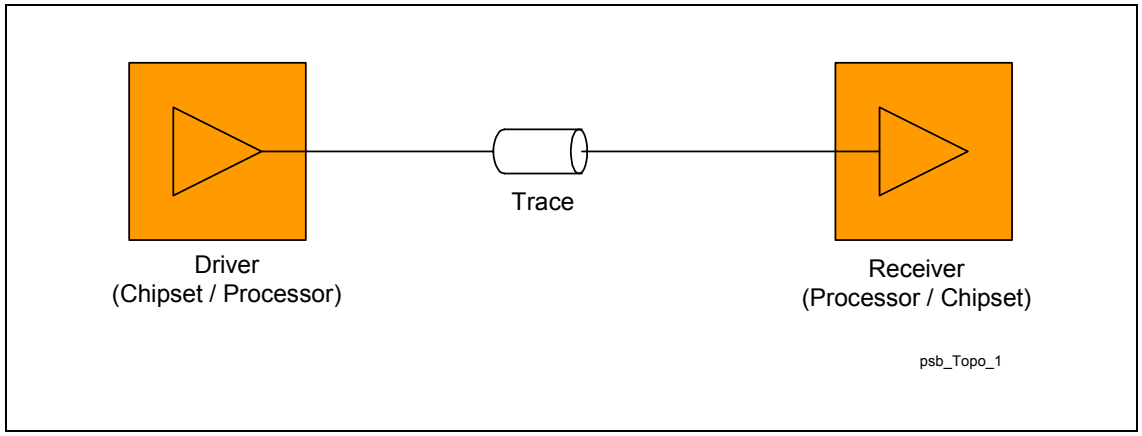
NOTE: Trace width of 5 mils and trace spacing of 10 mils within signal groups. Spacing between signal groups (address, data and control) should be 25 mils and for spacing from other (3.3 V) signals is 25 mils.

5.3.1. Topologies

5.3.1.1. Topology 1

Topology 1 requires that the signals be routed directly from the processor to the chipset. The processor has on-die termination, which removes the need for termination resistors on the motherboard.

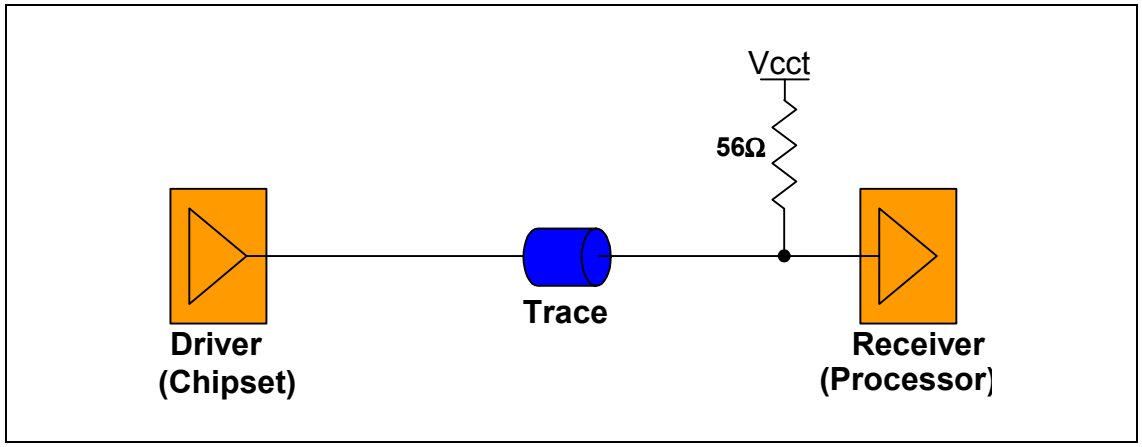
Figure 4. PSB Routing Topology 1



5.3.1.2. Topology 2

Topology 2 applies to only one signal; processor pin name RESET# and chipset ball name CPURST#. Topology 2 requires that there be a 56-Ω pullup to Vcct on the trace.

Figure 5. PSB Routing Topology 2



5.3.2. Trace Routing

Trace routing requires that the traces be routed in the inner layers (1.25 V power referenced) and via down to the bottom inner layer (within 500 mils) where they will be referenced to ground. There needs to be a capacitor near the via as there is a requirement of 1 capacitor for every three vias. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH.

5.3.3. Motherboard Layout Rules for AGTL Signals

5.3.3.1. Ground Reference

Intel recommends that AGTL signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

5.3.3.2. Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

5.3.3.3. CPU Connector Breakout

Intel strongly recommends that AGTL signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, breakout from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the CPU connector.

Following the above layout rules are critical for AGTL signal integrity, particularly for the 0.13-micron process technology.

5.3.3.4. Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high speed AGTL bus design:

1. Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
2. Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
3. Since AGTL is a low signal swing technology, it is important to isolate AGTL signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 3.3 V system memory.
4. Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
5. Route AGTL address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
6. Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
7. Minimize the dielectric process variation used in the PCB fabrication.
8. Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

5.3.4. Motherboard Layout Rules for Non-AGTL (CMOS) Signals

For all Non-AGTL (CMOS) signals, routing can be done on any layer or combination of layers.

Table 7. Routing Guidelines for Non-AGTL Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 8”
FERR#	5 mils	10 mils	1” to 8”
FLUSH#	5 mils	10 mils	1” to 8”
IERR#	5 mils	10 mils	1” to 8”
IGNNE#	5 mils	10 mils	1” to 8”
INIT#	5 mils	10 mils	1” to 8”
LINT[0] (INTR)	5 mils	10 mils	1” to 8”
LINT[1] (NMI)	5 mils	10 mils	1” to 8”
PICD[1:0]	5 mils	10 mils	1” to 8”
PREQ#	5 mils	10 mils	1” to 8”
PWRGOOD	5 mils	10 mils	1” to 8”
DPSLP#	5 mils	10 mils	1” to 8”
SMI#	5 mils	10 mils	1” to 8”
STPCLK#	5 mils	10 mils	1” to 8”

Table 8. Routing Guidelines for Non-AGTL Signals (for In-Target Probe)

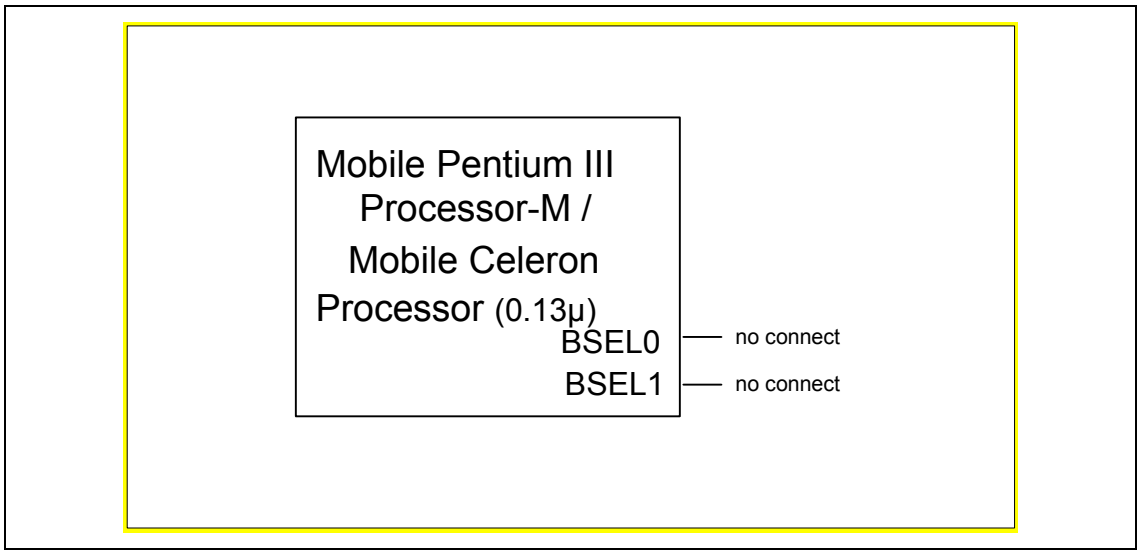
Signal	Trace Width	Spacing to Other Traces	Trace Length
TDI	5 mils	10 mils	1” to 8”
TDO	5 mils	10 mils	1” to 8”
TMS	5 mils	10 mils	1” to 8”
TCK	5 mils	10 mils	1” to 8”
TRST#	5 mils	10 mils	1” to 8”
PREQ#	5 mils	10 mils	1” to 8”
PRDY#	5 mils	10 mils	1” to 8”

5.4. BSEL[1:0] Implementation

These output signals are used to select the system bus frequency. The processor side bus frequency must be set to 100 MHz. All system bus agents must operate at the same frequency. Therefore, it is not required to connect BSEL lines since the processor drives these lines and does not use them as inputs. The BSEL lines are ignored and the clock generator is strapped to 100-MHz bus frequency. BSEL1

and BSEL0 signals on Mobile Pentium III Processor-M and Celeron processor (0.13 µ) may be left as no connect.

Figure 6. BSEL[1:0] Circuit Implementation



5.5. Undershoot/Overshoot Requirements

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and overshoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O Buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Mobile Pentium III Processor-M performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O Buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O Buffer model will impact results and may yield excessive overshoot/undershoot.

Refer to the latest *Mobile Intel® Pentium® III Processor-M Datasheet* and *Mobile Intel® Celeron® Processor(0.13µ) Datasheet* for more details.

5.6. Processor PLL Filter Recommendations

Intel mobile processors have an internal phase lock loop (PLL) clock generator, which are analog and require a quiet power supply to minimize jitter. Please refer to the *Mobile Pentium III Processor-M Datasheet* or *Mobile Intel® Celeron® Processor(0.13µ) Datasheet* for PLL specifications (see *Section 1.2* of this design guide for document references).

5.7. Voltage Regulation Guidelines

Please contact your Intel field sales representative for obtaining the guidelines.

5.8. Processor Decoupling Guidelines for Flexible Micro FCBGA Designs

This section contains decoupling guidelines for *flexible Micro-FCBGA* designs. Please refer to *Mobile Pentium III Processor-M Datasheet, Mobile Celeron Processor(0.13µ) Datasheet,* and specification updates for latest decoupling guidelines (see *Section 1.2* of this design guide for document references).

5.8.1. Vref Decoupling Design

Four 0.1-µF high frequency capacitors in a 0603 package placed near the Vref pins (within 500 mils).

5.8.2. Vcc_{CORE} Decoupling Design

High and Mid Frequency V_{CC} decoupling – Place twenty-four 0.22-mF 0603 capacitors directly under the package on the solder side of the motherboard using at least two vias per capacitor node. Ten 10-mF X7 6.3 V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.

The capacitors are arranged to minimize the overall inductance between V_{CC} / Vss power pins.

5.8.3. VccCORE Bulk Decoupling Design

Place Ten 150-µF Low-ESR tantalum capacitors close to the package. Via and trace guidelines are the same as above.

5.8.4. Vcct Decoupling Design

High and Mid Frequency V_{CCT} decoupling Place Ten 1-µF X5R/X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.

5.9. Thermal Considerations

Refer to the *Intel® 440MX PCISet Electrical and Thermal Specification Datasheet Addendum* and *Mobile Intel® Pentium® III Processor-M Datasheet,* and *Mobile Intel® Celeron® Processor (0.13µ) Datasheets* for platform thermal considerations.

6. System Memory Design Guidelines

6.1 Mobile DRAM Interface Overview

440MX integrates a main memory DRAM controller that supports a 64-bit DRAM array for mobile environments. Synchronous DRAM is the only memory type supported; Extended Data Out (EDO) memory is NOT supported. The DRAM interface operates at 100 MHz. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the 440MX BIOS Specification.

440MX supports industry-standard 64-bit wide, 144-pin SO-DIMM modules with SDRAM devices. Both symmetric and asymmetric addressing are supported. For write operations of less than a Qword in size 440MX performs byte-wide writes. 440MX supports 100 MHz SDRAM with CL2 or CL3 (CAS Latency of two or three), and supports one- and two- row SO-DIMMs. 440MX supports only self-refresh SDRAM. 440MX can be configured via the paging policy register to keep multiple pages open within the memory array. Pages can be kept open in all rows of memory. When using two-bank SDRAM devices in a particular row, up to 2 pages can remain open within that row.

440MX's DRAM interface is configured by the DRAM control registers, DRAM timing register, SDRAM control register, bits in the NBXCFG and four DRAM row boundary (DRB) registers. The DRAM configuration registers noted above control the DRAM interface to select RAS timing and CAS rates. The four DRB registers define the size of each row in the memory array, enabling 440MX to assert the proper CS# for accesses to the array.

6.1. DRAM Interface Signals

440MX's memory interface consists of the following signals:

- MA[13:0] Memory address signals
- MD[63:0] Memory data signals
- CS[3:0]# Chip select control signals
- DQM[7:0] Byte enable signals
- CKE[3:0] Clock enable signals
- SRAS# Row control signal
- SCAS# Column control signal
- WE# Write enable control signal

6.2. Mobile DRAM Layout Guidelines

- The DRAM expansion socket for mobile platforms is the 144-pin SO-DIMM.
- MA[11] should be connected to pin 106 of the SO-DIMM connector.
- MA[12] should be connected to pin 70 and pin 110 of the SO-DIMM connector.
- MA[13] should be connected to pin 72 and pin 112 of the SO-DIMM connector.

- For on-board 64Mbit SDRAM devices on the motherboard, MA[11] should be connected to A13/BA0 and MA[13] should be connected to A11 on the SDRAM device.
- The memory data byte lanes may be swapped to simplify board routing and minimize trace lengths (be sure to also swap the appropriate DQM signals). This can also be done for the data bits within a byte lane.
- Board impedance should be 55Ω ±15%.
- All resistors should be maximum 5% tolerance.
- Trace widths for memory signals should be 5 mil.
- Populate farther SO-DIMM first to avoid stub reflections.
- Any on-board memory should be located farther away from 440MX than a SO-DIMM connector.
- Place on-board DRAM and SO-DIMM connectors as near as possible to each other.

Figure 7 and Figure 8 provide two examples of routing the 440MX memory interface to on-board memory and SO-DIMM memory modules.

Figure 7. 440MX Memory Interface Routed to One or Two On-Board Memory Banks, One SO-DIMM Connector

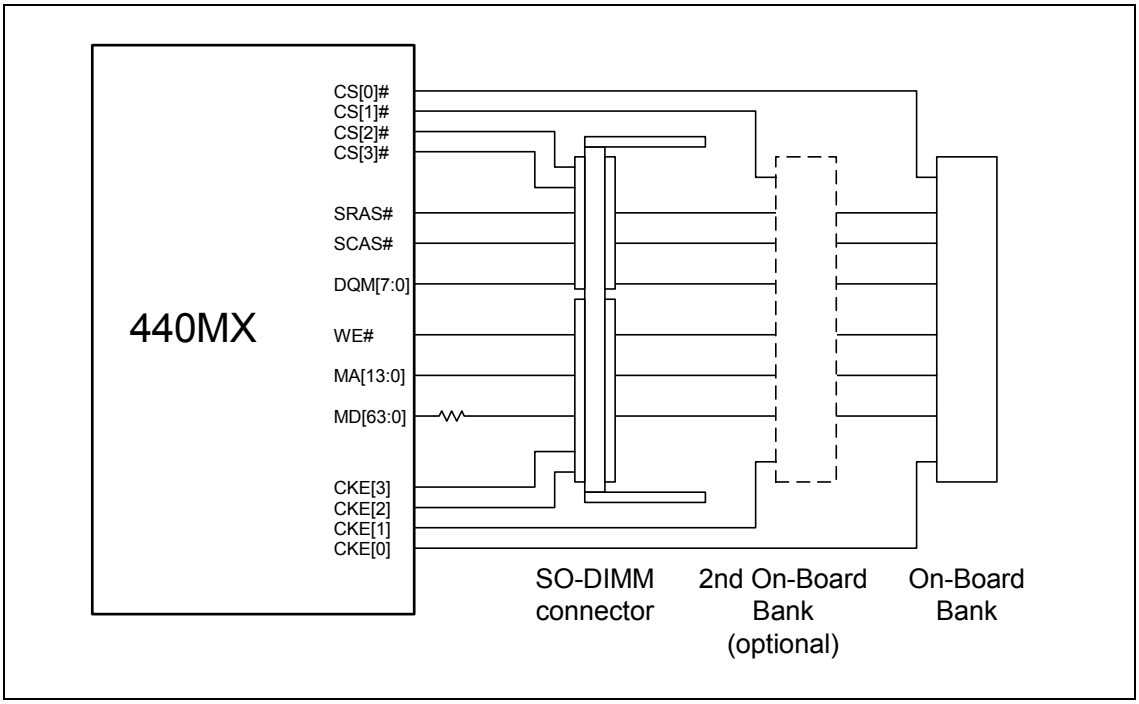
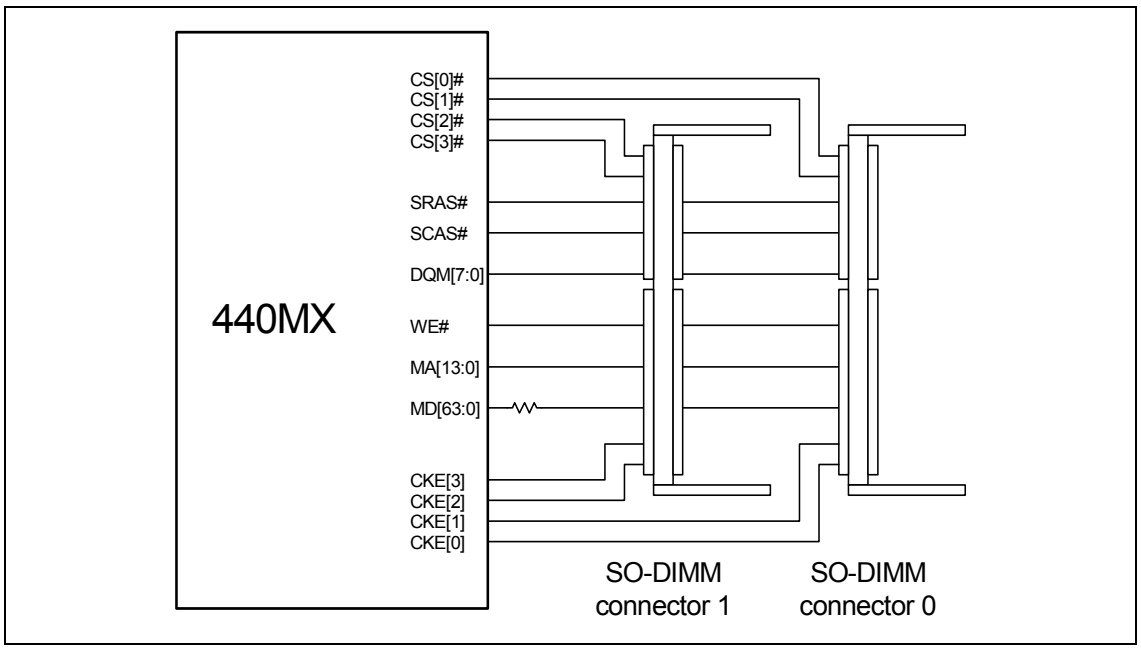


Figure 8. 440MX Memory Interface Routed to Two SO-DIMM Connectors



6.2.1. 100-MHz Memory Trace Lengths (With CK100 Clock Generator)

Memory traces should follow the guidelines set in the "Low-Power Module SDRAM DIMM Routing Guidelines" Application Note from January 2000, which are summarized in this section. Table 9 provides the minimum and maximum trace lengths to the SO-DIMM connector for each signal group (excluding clocks) for a CK100 design. Traces should be 55 Ω ± 10% and on inner layers 1:2 spacing. Trace widths should be 5 mils. For memory clock routing guidelines, see Section 6. System Memory Design Guidelines. Note that these guidelines are based on signal integrity and signal edge rates. A designer should evaluate whether resistors on additional signal(s) would be required for EMI or other concerns.

Table 9. SDRAM Interface Trace Lengths With CK100 Clock Generator

Signal	Min. Length		Max. Length		Damping Resistor
	(inches)	(mm)	(inches)	(mm)	
MA[13:0], WE#, SRAS#, SCAS#					
440MX to first slot	1.0	25.4	3.6	91.4	none required
between slots	0.0	0.0	0.6	15.2	none required
total length	1.0	25.4	3.6	91.4	none required
CKE[3:0]	1.0	25.4	3.25	82.5	none required
CS[3:0]#	1.0	25.4	4.0	101.6	none required
DQM[7:0]# (440MX to first slot)	1.0	25.4	4.0	101.6	none required

Signal	Min. Length		Max. Length		Damping Resistor
	(inches)	(mm)	(inches)	(mm)	
DQM[7:0]# (between slots)	0.0	0.0	1.0	25.4	none required
DQM[7:0]# (total length)	1.0	25.4	4.0	101.6	none required
MD[63:0] (440MX to damping resistor)	0.0	27.9	1.0	25.4	10Ω ±5%
MD[63:0] (from damping resistor to first slot)	1.0	25.4	4.0	101.6	
MD[63:0] (total length)	0.0	0.0	4.0	101.6	

The 440MX supports setting some options on power-up reset by strapping resistors on some MA lines (see Section 8.4.4 for details). Stubs created by routing to these pullup or pulldown resistors should be less than 0.1 inches (2.54 mm) in length.

7. Clocking Guidelines

7.1. Overview

This section provides clocking guidelines to be followed when routing signal traces for the board design. These guidelines are based on the HCLK, PCLK, and SDRAMCLK requirements and should be implemented along with the application instructions supplied by the clock vendor.

Signal routing order will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high-speed bus signals first. Either routing methodology can be used, provided the guidelines in this section are followed. If these guidelines are not followed, it is very important to simulate your design. Even when the guidelines are followed, it is still a good idea to simulate as many signals as possible for proper signal integrity, flight time and cross talk.

Note: This section applies to Mobile Pentium III Processor-M and Mobile Celeron Processor (0.13 µ).

7.2. Clocking Guidelines With CK100 Clock Generator

A CK100 compliant clock generator should be used to generate the system clocks for systems using a 100 MHz processor system bus and memory interface.

7.2.1. Clocking System Overview Option 1: CK100 Clock Generator With Integrated SDRAM Clock Buffer

Figure 9 shows the connections for a CK100 clock generator with integrated SDRAM buffer, LV/ULV Mobile Pentium III Processor-M, 440MX Chipset, SDRAM memory devices.

Figure 9. CK100 With Integrated SDRAM Clock Buffer - Clocking Block Diagram

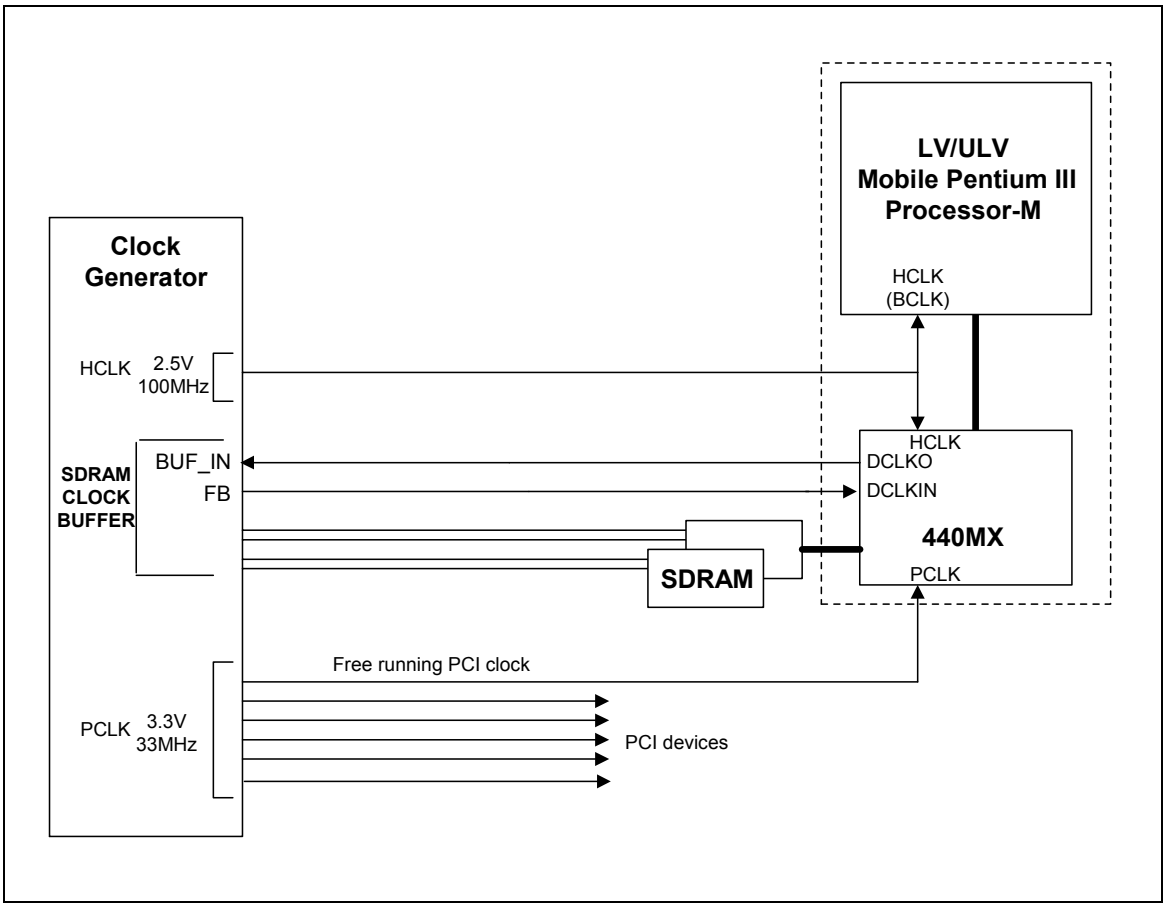
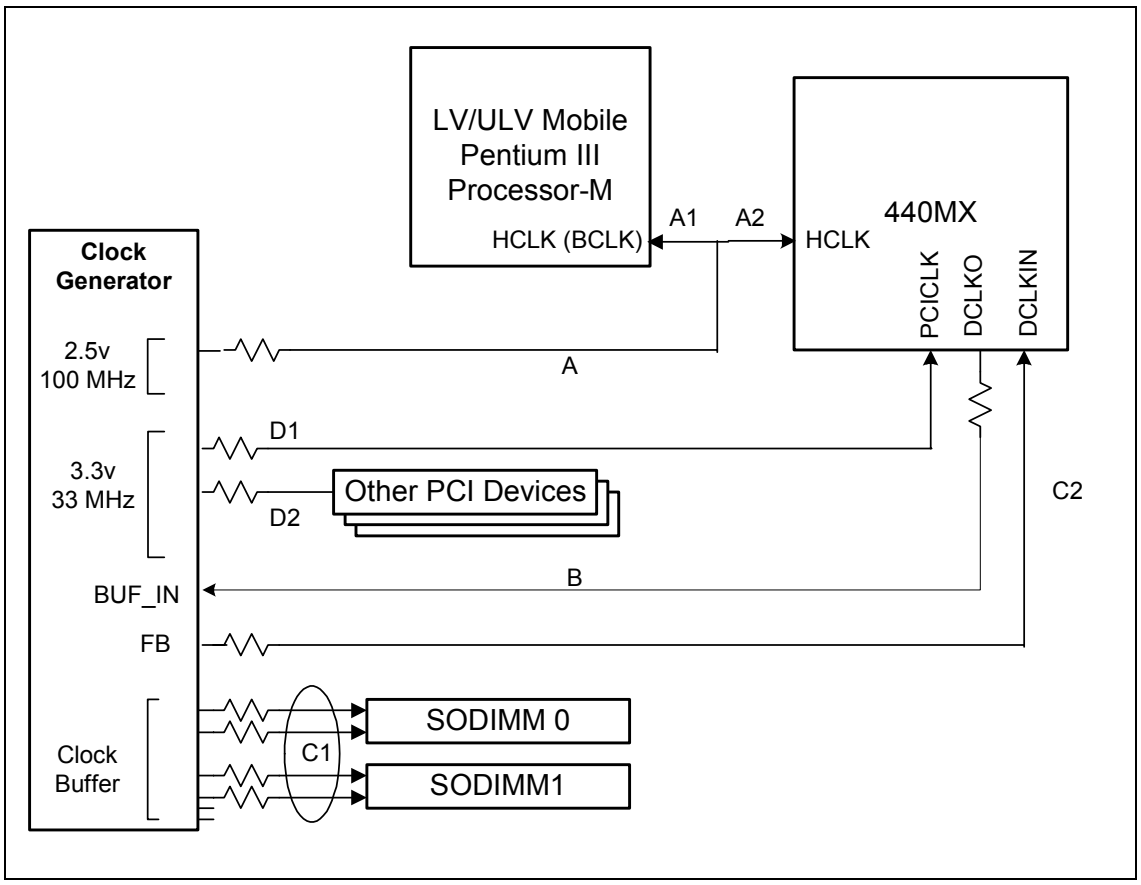


Figure 10. CK100 With Integrated SDRAM Clock Buffer - Clock Layout Guidelines of 440MX With LV/ULV Mobile Pentium III Processor-M at 100 MHz



** Refer to Section 7.4, *Clock Layout Guidelines for CK100 Clock Generators*. **

7.2.2. Specifications

A clock generator that meets *CK100 Clock Specification* will meet the requirement for a 440MX-based system. Section 7.7 lists clock vendors that will be providing clock synthesizers that meet CK100 Clocking Solution guidelines. The CK100 *Clock Specification* is available at http://developer.intel.com .

On CK100, Processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. CK100 also provides an integrated SDRAM clock buffer that provides clocks for SDRAM operating at 100 MHz at 3.3 V. For clock chip pinout information contact the preferred vendor in Section 7.7.

7.3. Clocking System Overview Option 2: Clocking Guidelines With CK100 Clock Generator and CKBF (Discrete SDRAM Clock Buffer)

A CK100 compliant clock generator should be used to generate the system clocks for systems using a 100-MHz processor system bus and memory interface.

7.3.1. Clocking System Overview With CK100-M Clock Generator

Figure 11 shows the connections for a CK100 clock synthesizer to the LV/ULV Mobile Pentium III Processor-M, the 440MX Chipset, and SDRAM devices and/or slots.

Figure 11. CK100 With Discrete SDRAM Clock Buffer - Clocking Block Diagram

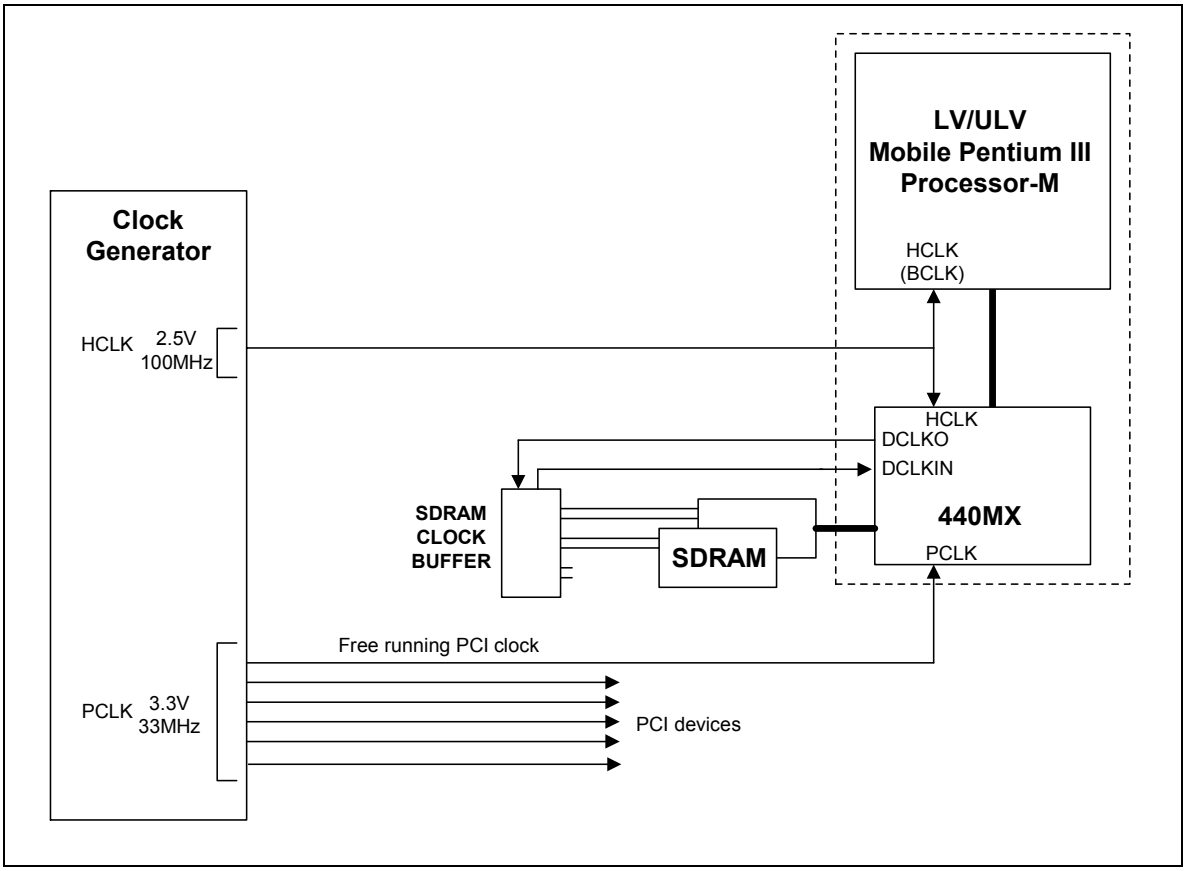
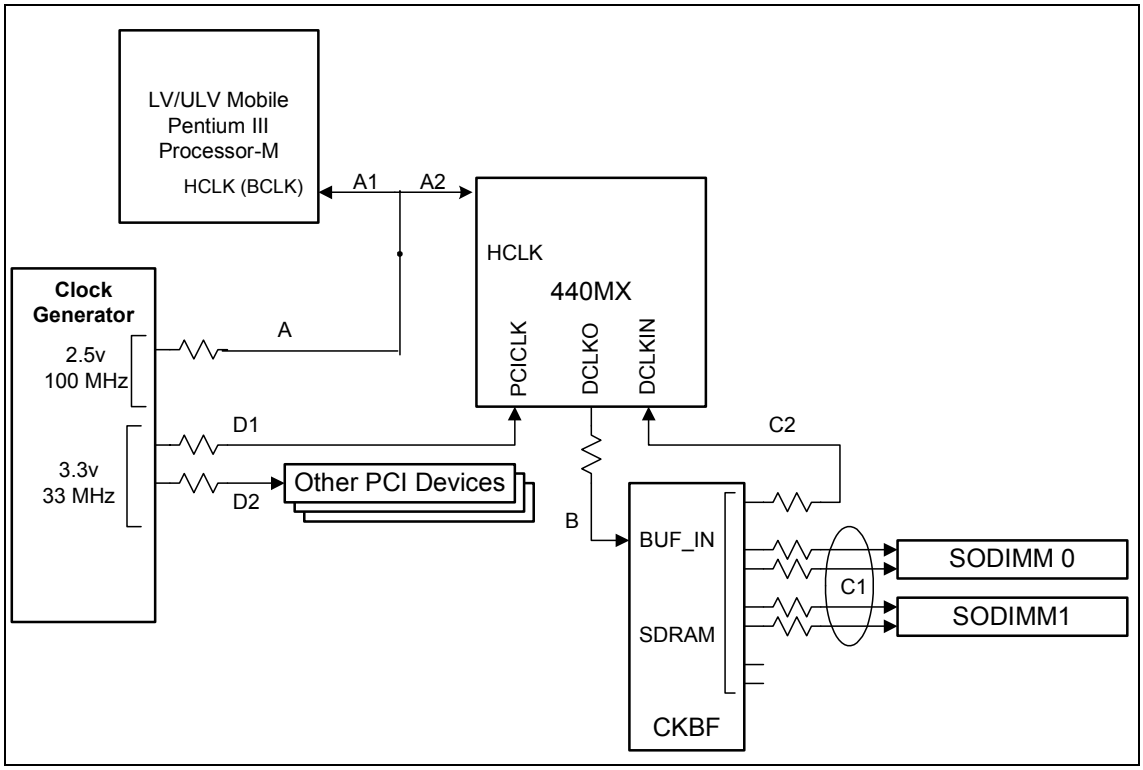


Figure 12. Clock Layout Guidelines of 440MX Chipset With LV/ULV Mobile Pentium III Processor-M at 100 MHz



** Refer to Section 7.4, *Clock Layout Guidelines for and CK100 Clock Generators*. **

7.3.2. CK100 Clock Synthesizer Pinout and Specifications

A clock synthesizer that meets *CK100 Clock Specification* will meet the requirement for a 440MX based system. Section 7.7 lists clock vendors that will be providing clock synthesizers that meet CK100 Clocking Solution guidelines. The *CK100 Clock Specification* can be obtained from your Intel field representative.

Note: The CK100 is running in the multi-voltage mode. The processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. The CKBF provides clocks for SDRAM operating at 100 MHz at 3.3 V.

Figure 13. Pinout for CK100 Clock Synthesizer (With No Clock Buffer)

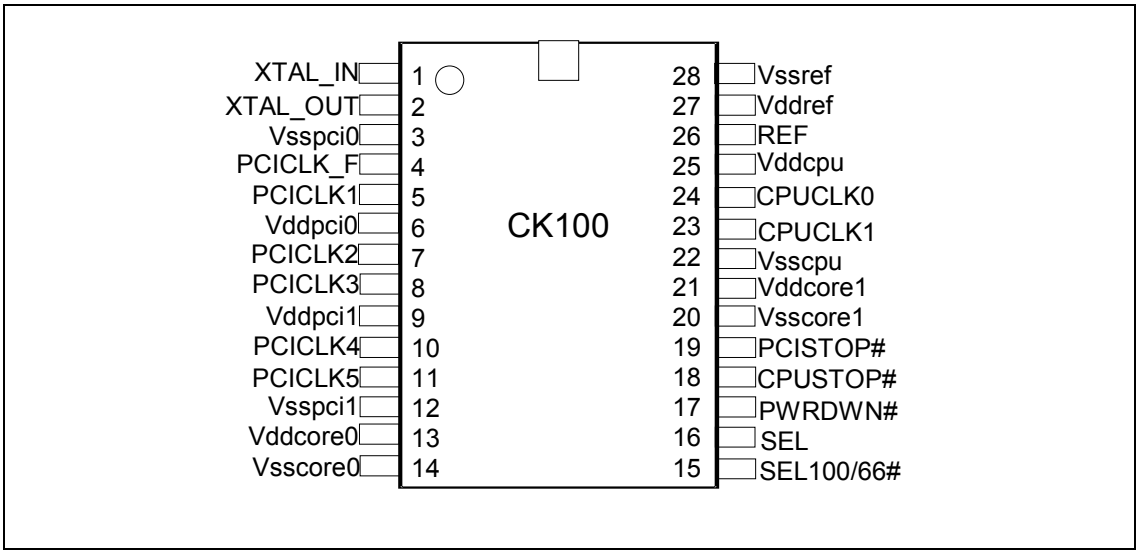
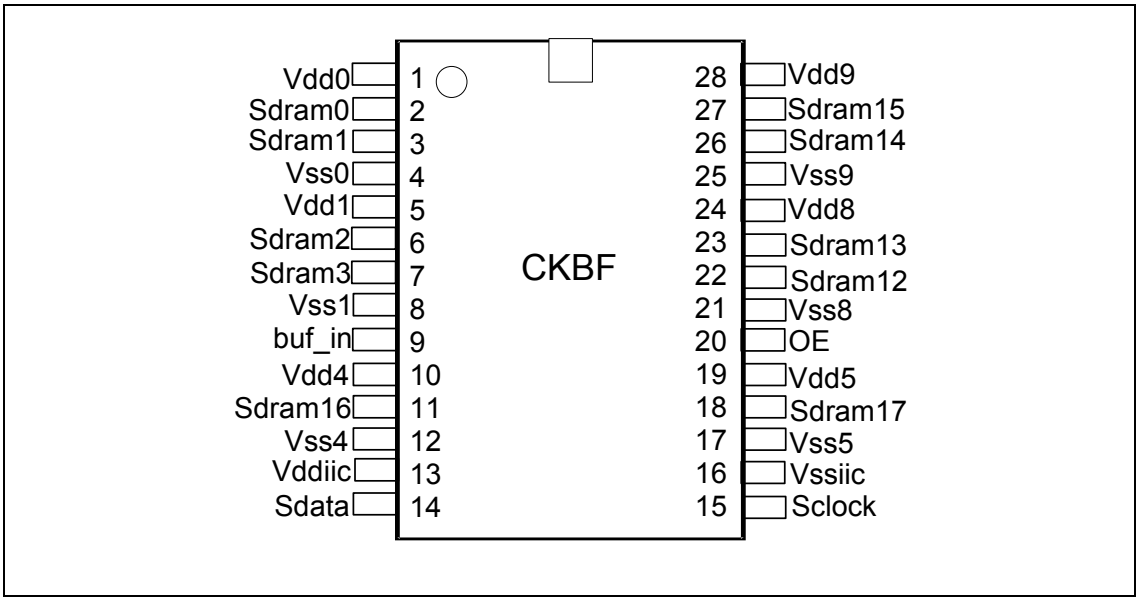


Figure 14. Pinout for CKBF Clock Buffer



7.4. Clock Layout Guidelines for CK100 Clock Generators

Note that these guidelines are for illustration purposes; it is up to an individual designer to ensure that all timing and signal quality requirements for the chipset, processor, and memory devices are met.

1. For each clock signal where the trace transitions from the surface layer to an internal layer, place a ground via stitching the two ground planes together.
2. General guidelines:
   - All clocks except CPUCLKs should be routed 55 Ω ±10% with 1:2 spacing.
   - Minimize the use of vias on clock signals.
3. To minimize cross-talk:
   - Clock trace spacing is recommended to be at least 14 mil.
   - Serpentine trace separation should be a minimum of 18 mil.
4. Series matching resistors are required as near to the driver pin as possible (less than 1”). See (Table 11) 440MX Strapping Options for values.
5. A PCICLK that is used for a PCI socket or is sent to a docking station should be implemented as a point-to-point connection and not be shared with another load.
6. If designing with docking connector, remember to account for the PCICLK trace length in the docking station.
7. Place all damping resistors and filter capacitors < 0.5” to clock generator.
8. Place all decoupling caps close to clock generator.
9. Route all clocks on internal layers to provide better trace delay consistency as well as EMI containment.
10. Board impedance should be 55Ω ±15%
11. Use discrete resistors on HCLK signals coming from the clock generator.
12. For CK100 with CKBF: CKBF should be on V3 rail and CK100-M should be on the V3S rail.

Table 11. LV/ULV Mobile Pentium III Processor-M / 440MX Chipset Based System: Clock Trace Length and Width Specifications

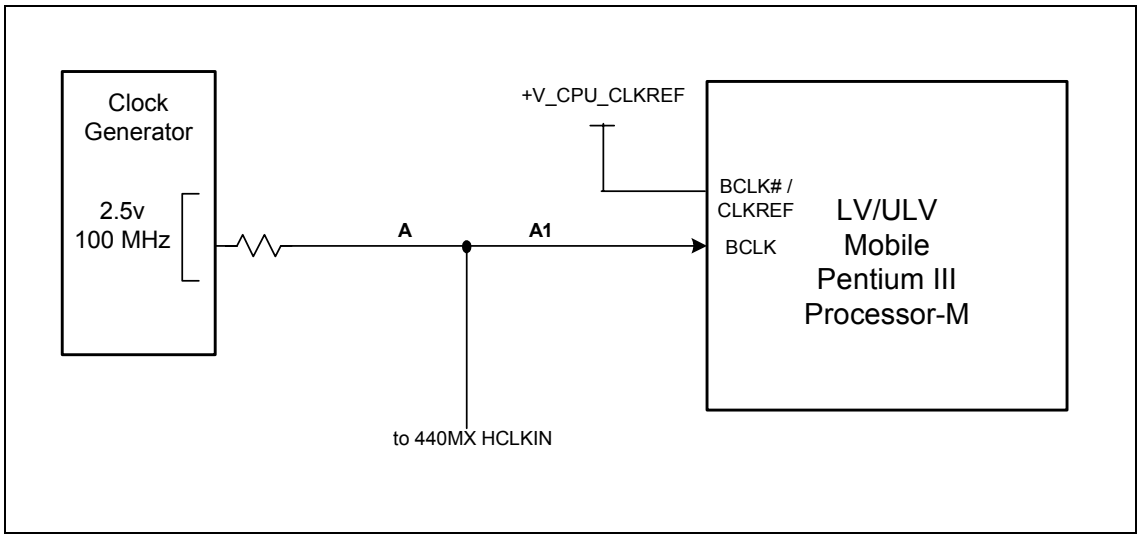
Variable	Trace Length (min)	Trace Length (max)	Tolerance(2)	Trace Width	Resistor
A	2.0 inches (50.8 mm)	4.5 inches (114.3 mm)		8 mil	22 Ω ±5%
A1	A2 + 0.876 inches (A2 + 22.25 mm)	A2 + 0.878 inches (A2 + 22.30)		4 mil	NONE
A2	1.25 inches (31.8 mm)	1.35 inches (34.3 mm)		4 mil	NONE
B	0	4.0 inches (101.6 mm)		5 mil	18 Ω ±5%
C1	0	4.0 inches (101.6 mm)	+/- 0.1 inch (+/- 2.54 mm)	5 mil	18 Ω ±5%
C2 (Note 1)	C1 + 2.4 inches (C1 + 60.9 mm)	C1 + 2.6 inches (C1 + 66 mm)		5 mil	18 Ω ±5%
D1	A + A2	A + A2 + 4.0 inches (A + A2 + 101.6 mm)		5 mil	33 Ω ±5%
D2	D1	D1	+/- 4.0 inches (+/- 101.6 mm)	5 mil	33 Ω ±5%

NOTES:

1. For platforms with on-board memory devices, clock traces should be routed as if there were a “phantom” connector on the board. The designer should follow the routing guidelines in the *66/100 MHz Unbuffered SDRAM 64-bit Non-ECC/Parity 144-pin SO-DIMM Specification* for the clock signals from the “phantom” connector to the on-board memory devices. In other words, route the clock trace to the position that SODIMM0 would occupy following the constraints given above, and route from that point onward according to the *66/100 MHz Unbuffered SDRAM 64-bit Non-ECC/Parity 144-pin SO-DIMM Specification*.
2. “Tolerance” refers to the allowed difference in length between multiple traces sharing the same variable name.

7.5. Single-Ended LV/ULV Mobile Pentium III Processor-M Clocking

Figure 15. LV/ULV Mobile Pentium III Processor-M - Single-Ended Clocking Block Diagram



** Refer to Section 7.4, *Clock Layout Guidelines for CK100 Clock Generators*. **

7.6. Optional Clock Layout

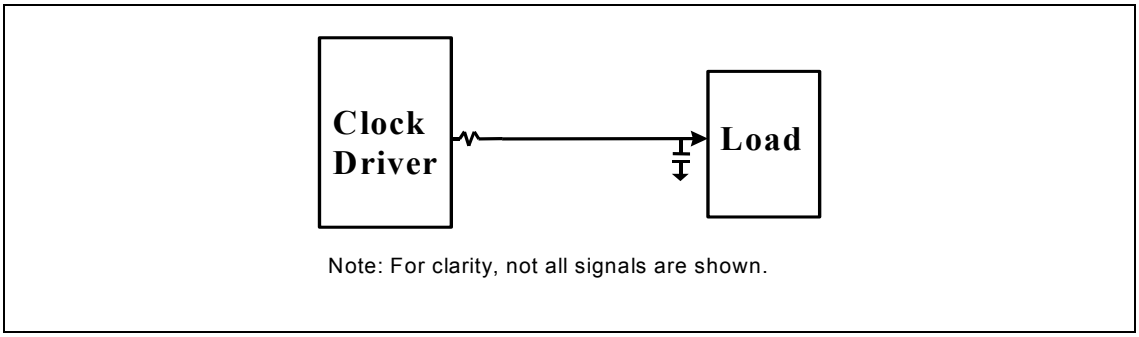
Figure 16 illustrates an optional clock layout implementation to accommodate tuning of HCLK, SDRAMCLK, and PCLK clocks from CK100 Generators. This allows tuning individual clock signals to minimize EMI and allow for variations in impedance, skew and loading. Refer to the *Intel® Mobile EMI Design Guide*.

The variables to be considered include:

- Variation in actual device load
- Line and load impedance variation
- Driver output impedance
- Vendor variation

Minimize the stub to the capacitor. The maximum stub length on a clock trace is < 0.5 inches. The capacitor should be placed as close as possible to the load. Refer to the clock vendor specifications for layout and termination guidelines.

Figure 16. General Clock Layout



7.7. Clock Vendors*

Integrated Circuit Systems, Inc.*
1271 Parkmoor Avenue
San Jose, CA. 95126-3448
(408) 925-9460

Cypress Semiconductor Corporation*
3901 North First Street
San Jose, CA 95134
(408) 943-2600

*Companies and/or products are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality or compatibility of these companies and/or product. This list may be subject to change without notice. Listed companies and products in no way constitute a recommendation of products or companies by Intel, but rather indicate a potential source for products and/or companies. Other companies may offer additional products of interest.

8. Design Review Checklists

8.1. Overview

The checklists in this section are intended for schematic reviews of 440MX and LV/ULV Mobile Pentium III Processor-M-based platform designs. It does not represent the only way to design the system, but does provide our recommendations. The system designer should examine the checklist items for accuracy.

Pull up and pulldown resistor values are system dependent. The appropriate value for a specific system can be determined from an AC/DC analysis of the pullup voltage, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pullup voltage tolerance, the pullup/pulldown resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. To determine the optimal value, cost concerns, commonality considerations, manufacturing issues, specifications and other considerations must be evaluated.

Simplistic DC calculations for pullup values can be performed using the following equations:

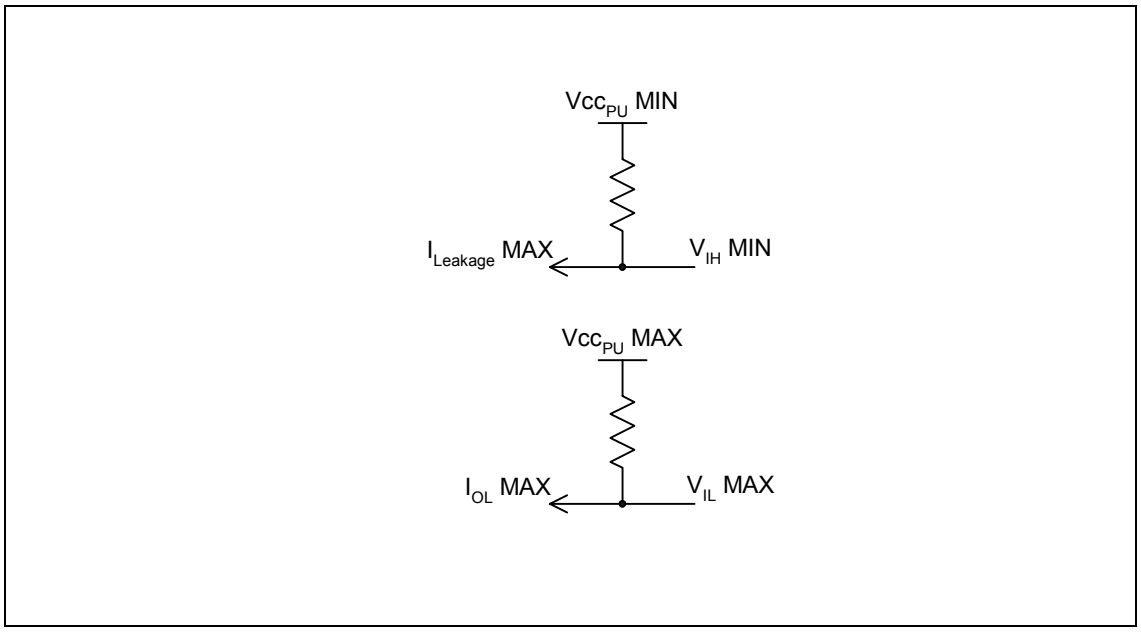
Equation 1.

$$R_{MAX} = (V_{CCPU}\ MIN - V_{IH}\ MIN) / I_{Leakage}\ MAX$$

$$R_{MIN} = (V_{CCPU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Figure 17 shows an example of the minimum and maximum pull-up resistor configurations.

Figure 17. Pullup Resistor Example



8.2. LV/ULV Mobile Pentium III Processor-M and LV/ULV Mobile Celeron Processor (0.13 µ)

This section provides design requirements specific to the LV/ULV Mobile Pentium III Processor-M and Mobile Celeron Processor (0.13 µ). Refer to Section 8.4.7 for information pertaining to the interfaces between the chipset and processor.

8.2.1. LV/ULV Mobile Pentium III Processor-M Errata and LV/ULV Mobile Celeron Processor (0.13 µ) Errata

Please see the *Mobile Intel® Pentium® III Processor-M Specification Update* and the *Mobile Intel® Celeron® Processor (0.13µ) Specification Update* for workarounds of any errata that may be present for a particular stepping.

8.2.2. Power and Ground Pins

The following voltage planes supply power to the LV/ULV Mobile Pentium III Processor-M, LV/ULV Mobile Celeron Processor (0.13 µ) or its interfaces:

- V_{CC} pins supply power to the processor core logic.
- V_{CCT} supplies voltage for the processor AGTL interface including the internal pullup resistors.
- 1.5 V (V_{CCT_IO}) supplies power to the processor sideband signals, though this voltage is not supplied directly to the processor core.
- V_{REF} pins provide a reference voltage for the processor AGTL interface. V_{REF} is also supplied to the 440MX. See Figure 18 and Table 10 for reference voltages.
- CMOSREF provides a reference voltage for CMOS input buffers.
- CLKREF provides a reference voltage to define the trip point for the BCLK signal.
- The voltage ID signals (VID[4:0]) should have pullup resistors connected to a power supply that is guaranteed to be stable when power to the core is stable.
- The LV/ULV Mobile Pentium III Processor-M does not require a 3.3-V supply.

Refer to the *Mobile Intel® Pentium® III Processor-M Datasheet and Mobile Intel® Celeron® Processor (0.13µ) Datasheet* for a list of power, ground, test, and reserved / no connect pins as well as precise values and tolerances for these voltage planes.

Figure 18. Circuit for Generating Reference Voltages

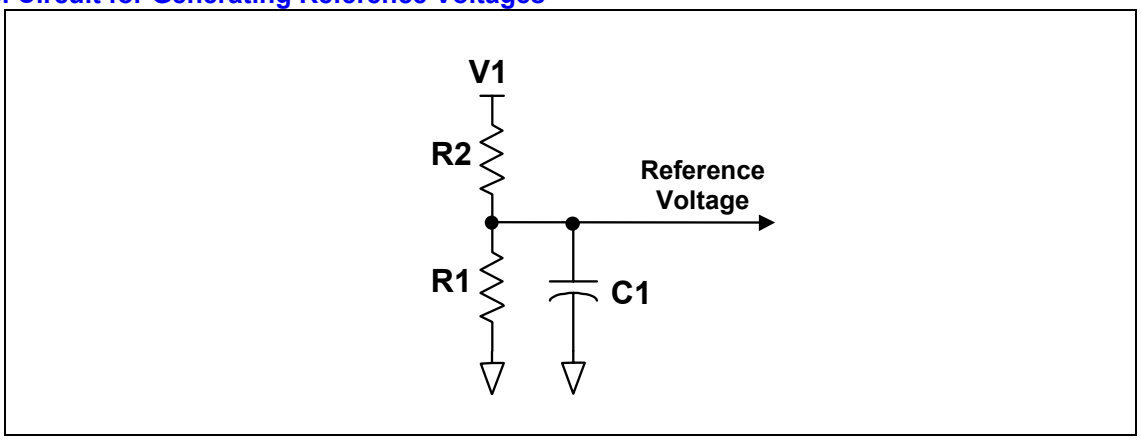


Table 10. Values for Reference Voltages*

Reference Voltage	Target Voltage (V)	V1 (V)	R1 (kΩ) (recommended)	R2 (kΩ) (recommended)	Tolerance (each resistor)	C1 (µF)
V_{REF}	$2/3V_{CCT}$	V_{CCT_IO} (1.5V)	2	1	1%	4 - 0.1
CMOSREF	1.00	V_{CLK}	1	1.5	1%	2 – 0.1
CLKREF	1.25	V_{CLK}	1	1	1%	1

NOTES: * Notes on reference voltage circuits:
1. VREF - place resistors between chipset and processor. Place decoupling caps near processor.
2. CMOSREF – place decoupling caps near processor.
3. CLKREF – place entire circuit near BCLK# (CLKREF) pin of LV/ULV Mobile Pentium III Processor-M or LV/ULV Mobile Celeron Processor (0.13 µ).

8.2.3. Decoupling Guidelines

1. The amount of bulk decoupling required to meet the voltage tolerance requirements for the LV/ULV Mobile Pentium III Processor-M or LV/ULV Mobile Celeron Processor (0.13 µ) is a strong function of the power supply design. See *Section 5.8* of this document for processor decoupling recommendations.
2. The Low Power AGTL voltage reference power plane (V_{REF}) should have at least four 0.1 µF high frequency decoupling capacitors.
3. The Low Power CMOS reference power plane ($CMOS_{REF}$) should have at least two 0.1 µF high frequency decoupling capacitors.
4. The Low Power 2.5-V reference power plane (CLK_{REF}) should have at least one 1-µF high-frequency decoupling capacitor.

8.1.1 Clock and Test Signals

1. See Section 7. Clocking Guidelines for more information.
2. Ensure that the clock generation logic to the LV/ULV Mobile Pentium III Processor-M and LV/ULV Mobile Celeron Processor (0.13 µ) is at 2.5 V (BCLK, PICCLK (if used), and TCK (if used)).
3. All reserved pins must be unconnected.

4. TESTHI_0 and TESTHI_1 are for testing only; pull each signal up to V_{CCT} using discrete 1-kΩ resistors.
5. TESTLO_0 and TESTLO_1 signals are for testing only; tie each of these signals to V_{SS} through discrete 1-kΩ resistors.

8.2.4. LV/ULV Mobile Pentium III Processor-M and LV/ULV Mobile Celeron Processor (0.13 µ) Signals

1. Refer to Section 8.4.6 and Section 8.4.7 for design information on the processor system bus interface and the processor side-band signals, respectively.
2. Ensure that the processor inputs are not being driven by 3.3-V or 5-V logic. Logic translation of 3.3V or 5V signals may be accomplished by using open-drain drivers pulled-up to the appropriate voltage.
3. All RESERVED and NO CONNECT pins must be unconnected.
4. Unused CMOS active low inputs should be connected to V_{CCT_IO} through 1.5-kΩ resistors and unused active high inputs should be connected to V_{SS} through 1-kΩ resistors. Unused CMOS outputs may be left unconnected.
5. Due to on-die Rtt resistors on the processor, additional resistors do not need to be placed on the motherboard for most PSB signals. The lone exception is on the CPURST# signal which requires a 56-Ω pullup to Vcct on the processor end of the transmission line.
6. The processor includes a signal, EDGCTRLP, to configure the edge rate of the Low Power AGTL output buffers. Connect EDGCTRLP to V_{SS} with a 110 Ω, 1% resistor.
7. Processor output signals BSEL[1:0] can drive the clock generator to set processor system bus speed. It is NOT required to drive the BSEL lines since 100 MHz is the only supported processor side bus frequency using Mobile Pentium III Processor-M or Mobile Celeron Processor (0.13 µ) with the 440MX Chipset. Leave signals BSEL1 and BSEL0 unconnected.
8. The processor implements an ITP port supporting the IEEE JTAG specification. TDI should have only one 200 Ω pullup to VCCT_IO (1.5V) if it is being used. If it is not used then it should have a 1-kΩ pulldown resistor. TCK should have a 39 Ω pull down and TMS should have a 39 Ω pullup to 1.5V if they are being used. If they are not used, then they should have a 1-kΩ pulldown resistor. TRST# should have only one 500-Ω pulldown whether or not it is being used.
9. PWRGOOD is a 1.8-V tolerant input. It is expected that this signal will be a clear indication that clocks and the power supplies (V_{CC}, V_{CCT}, V_{CCT_IO}, etc.) are stable and within their specifications. Intel highly recommends that the PWRGOOD signal from the power supply **not** be connected directly to logic on the board without first going through a Schmitt trigger type circuitry to square-off and maintain the signal integrity of PWROK.
10. The LV/ULV Mobile Pentium III Processor-M and LV/ULV Mobile Celeron Processor (0.13 µ) currently requires the CPU APIC to be hardware enabled. PICCLK must be driven with a clock that meets specification and the PICD[1:0] signals must be pulled up to $1.5V$ with 150Ω resistors, even if the local APIC is not used.
11. At reset, the state of the A15# signal must be driven low to configure the processor for Quick Start state. 440MX will drive this signal to the correct value.
12. The LV/ULV Mobile Pentium III Processor-M has specific power sequencing requirements. Refer to the Mobile Pentium III Processor-M and Mobile Celeron Processor (0.13 µ) Datasheet for details.

8.3. Design Comparisons Implementing LV/ULV Mobile Intel Pentium III Processor Versus LV/ULV Mobile Pentium III Processor-M

1. On LV/ULV Mobile Pentium III Processor-M, a 56-Ω pullup on processor RESET# is required.
2. LV/ULV Mobile Pentium III Processor-M uses AGTL Reference Voltage at 1.25 V. Layout topology requirements for AGTL signals differ from LV/ULV Mobile Pentium III processor. LV/ULV Mobile Pentium III Processor-M AGTL signals should be 5 on 10 (5 mils wide, 10 mils spacing) and routed 2 to 4 inches in length. See Section 5.3 of this document for more details on LV/ULV Mobile Pentium III Processor-M routing and topology guidelines.
3. Processor core decoupling: See Section 5.8 for general guidelines on LV/ULV Mobile Pentium III Processor-M decoupling.
4. On LV/ULV Mobile Pentium III processor, the IOAPIC interface was disabled by pulling signals (PICCLK and PICD[1:0]) to ground through resistors. The LV/ULV Mobile Pentium III Processor-M requires the CPU APIC to be hardware enabled. PICCLK must be driven with a clock that meets specification and the PICD[1:0] signals must be pulled up to 1.5V with 150-Ω resistors, even if the local APIC is not used.
5. For LV/ULV Mobile Pentium III Processor-M In-Target Probe (ITP) connectivity: TDI should have only one 200 Ω pullup to V_{CCT_IO} (1.5V) if it is being used. If it is not used then it should have a 1-kΩ pulldown resistor. TCK should have a 39-Ω pull down and TMS should have a 39-Ω pullup to 1.5V if they are being used. If they are not used, then they should have a 1-kΩ pulldown resistor. TRST# should have only one 500-Ω pulldown whether or not it is being used.

8.4. 440MX Design Checklist

This section provides 440MX Chipset design information.

8.4.1. 440MX Errata

Please see the 440MX Specification Update for workarounds of any errata that may be present for a particular stepping.

8.4.1.1. Modem Recommendations for 440MX Low Power Platforms

PCI modem implementations are recommended for platforms that require fully optimized battery life. 440MX Specification Update Errata #34 forces Intel SpeedStep Technology to be disabled when an active AC'97 modem is detected. Errata #34 also forces Enhanced Intel SpeedStep Technology to be disabled when an active AC'97 modem is detected. Enhanced Intel SpeedStep Technology is a new battery life enhancement that relies on Intel SpeedStep Technology transitions.

Platforms that do not require fully optimized battery life can use either AC'97 or PCI modem implementations. For platforms that implement AC'97 modem:

- Platform power state will be frozen when the modem is detected to be active. The system will remain in a fixed power state.
- The power state will be either Performance Mode or Battery Optimize Mode.

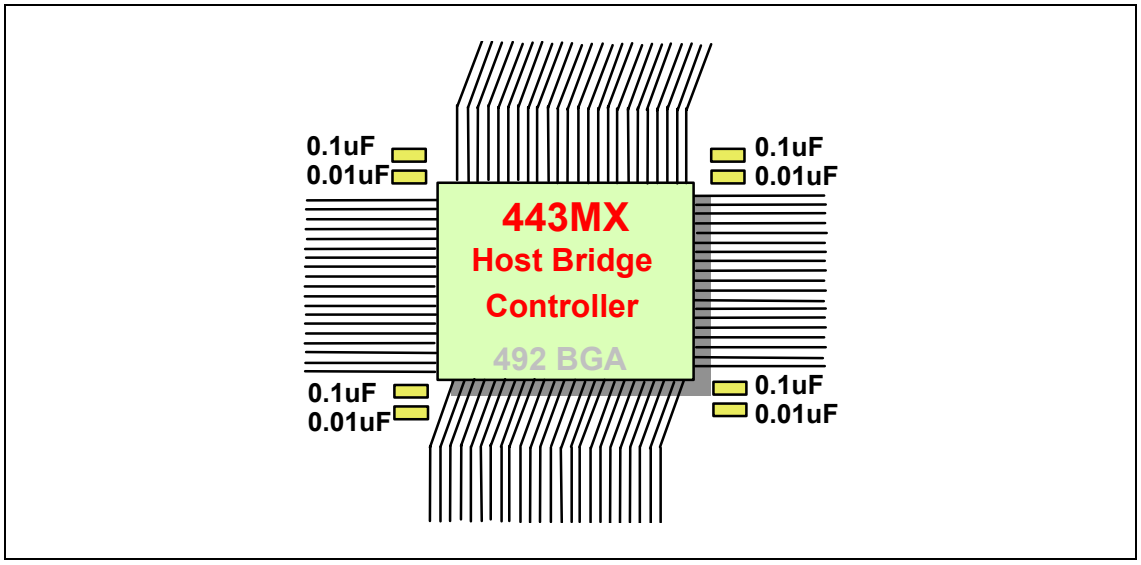
8.4.2. 440MX Power and Ground Pins

1. Power plane terminology is included here for use with the recommendations provided in this section.
   - *V3 is a 3.3-V power plane controlled by SUSC#. It is on during power-on suspend (POS, ACPI S1 or S2), suspend-to-RAM (STR, ACPI S3), and off in suspend-to-disk (STD, ACPI S4) and soft-off (SOFF, ACPI S5).*
   - *V3S is a 3.3-V power plane controlled by SUSB#. It is on during POS and off in STR, STD, and SOFF.*
   - *V5 is a 5-V power plane controlled by SUSC#. It is on during POS and STR, off in STD and SOFF.*
   - *V5S is a 5-V power plane controlled by SUSB#. It is on during POS and off in STR, STD, and SOFF.*
   - *V3RSM is a 3.3-V power plane that is on whenever 440MX's resume logic is active.*
   - *V3RTC is a power plane that supplies power to 440MX's real time clock and CMOS RAM. It should always be on to maintain power to the RTC and CMOS RAM.*
   - *V_{CCT_IO} supplies power to the processor side band signals; it is not directly supplied to 440MX.*
2. 440MX V_{CC}(CORE) pins provide power to the core logic; supply with V3.
3. 440MX V_{CC}(USB) pins supply power to the USB host controller; supply with V3RSM. Can also use V3, but ensure the power supplied to V_{CC}(USB) is clean.
4. 440MX V_{CC}(RSM) pins supply power to the resume logic; supply with V3RSM.
5. 440MX V_{CC}(RTC) supply power to the RTC and CMOS RAM circuitry; supply with V3RTC.
6. 440MX V_{5REF} is a 5-V reference voltage. V_{5REF} must be tied to 5V in a 5V tolerant system. This signal must be powered up before or simultaneous to V_{CC}(CORE), and it must be powered down after or simultaneous to V_{CC}(CORE). Note that since V_{CC}(CORE) is powered by V3, V_{5REF} should be powered by V5 and not V5S. V_{5REF} can be tied to V_{CC}(CORE) in a non 5-V tolerant system; however, note that currently most IDE drives are 5-V only.
7. If additional AGTL termination is required (i.e. a logic analyzer connector is used), supply with V_{CCT} (same as processor AGTL voltage).
8. V_{REF} is a reference voltage for the AGTL interface and can be shared with the V_{REF} for the processor.

8.4.3. 440MX Decoupling Guidelines

Decoupling capacitors should be placed at the corners of the 440MX mBGA package (see Figure 19). A minimum of four to eight 0.1-µF capacitors with four to eight 0.01-µF or 0.001-µF capacitors should be used, depending on how quiet the system's power planes are and other specific EMI considerations.

Figure 19. 440MX Decoupling



NOTE: ** There are other discrete components for V_{CCT_IO}, AGTL Ref Voltages that must be also considered when routing around 440MX.

8.4.4. 440MX Strapping Options

Table 11. 440MX Strapping Options

Pin Name	Function	Low	High	Internal Resistor	Status Register
MA12#	System frequency select	66MHz	100MHz	pulldown	NBXCFG[13]
MA11#	In-Order Queue Depth Enable	1 (no pipelining)	4 (max)	pullup	NBXCFG[2]
MA10	Quick Start Select	Stop Clock Mode	Quick Start Mode	pullup	PMCR[3]
MA8#	Reserved			pulldown	
MA13#	CPU clock ratio: sets NMI	NMI low	NMI high	pulldown	
MA9#	CPU clock ratio: sets INTR	INTR low	INTR high	pulldown	
MA7#	CPU clock ratio: sets IGNNE#	IGNNE# low	IGNNE# high	pulldown	
MA1#	CPU clock ratio: sets A20M#	A20M# low	A20M# high	pulldown	

NOTES:
1. Internal resistors are 50-kΩ pullup or pulldown.
2. Use external resistors of 10 kΩ to configure modes.
3. Strapping option pullups should be to V3.
4. This document assumes MA12# has a pullup enabling 100-MHz operation.

The mobile processor bus ratio is programmed into the processor during manufacturing and cannot be overridden.

8.4.5. 440MX Clock and Test Signals

1. See Section 7. Clocking Guidelines for more information.
2. Do not mix HCLK, PCICLK, and SDRAMCLK signals coming from the CK100 devices in R-packs; use discrete resistors.

3. USB Clock - 48 MHz with a duty cycle of better than 40/60% should be fed into 440MX's USB clock input.
4. TEST# is in the resume well (not RTC well). Pull high to V3RSM with a 10kΩ resistor.

8.4.6. Processor System Bus (PSB)

1. Termination of the Low Power AGTL bus is not necessary for the LV/ULV Mobile Pentium III Processor-M or LV/ULV Mobile Celeron Processor (0.13 µ) unless a logic analyzer connector is present.
2. All unused Low Power AGTL signals should be left unconnected.
3. Note that processor address and data bus signals are logically inverted signals. The actual values are inverted from what appears on the processor bus.

8.4.7. Processor Side-Band Signals

1. The processor side-band signals require pullup resistors as indicated in Table 12. Note that unused inputs should be pulled to their inactive values. Unused outputs may be left unconnected.
2. Since the side-band signal FERR# is an input to the 440MX, it needs to be voltage translated using a FET or PNP transistor. One method of this is shown in Figure 20.

Figure 20. Voltage Translation of FERR#

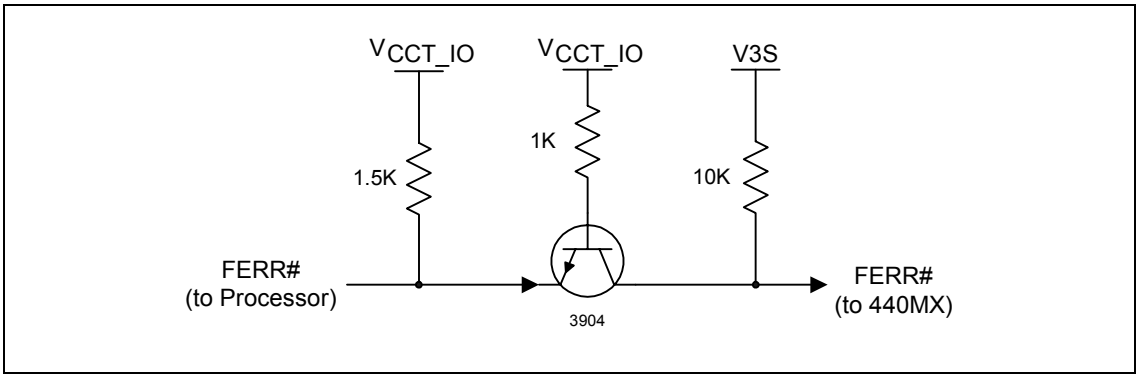


Table 12. Processor Side-Band Signals

Signal	Function	Pullup / Pulldown Resistor	Notes
A20M#	Address 20 Mask	1.5 kΩ pullup to V_{CCT_IO}	Connect to 440MX
FERR#	Floating Point Error	1.5 kΩ pullup to VCCT_IO on processor side of FET	Requires voltage translation – use a FET. 440MX side of FET requires 10k pullup to +V3S
FLUSH#	Flush	3 kΩ pullup to V_{CCT_IO}	Not supported by 440MX
GHI#	Intel SpeedStep Technology	None	Pullup internal to processor
IERR#	Internal Error	1.5 kΩ pullup to V_{CCT_IO}	Not supported by 440MX; pullup resistor is optional
IGNNE#	Ignore Numeric Error	1.5 kΩ pullup to V_{CCT_IO}	Connect to 440MX
INIT#	Initialization	1.5 kΩ pullup to V_{CCT_IO}	
INTR	Interrupt	1.5 kΩ pullup to V_{CCT_IO}	
NMI	Non Maskable Interrupt	1.5 kΩ pullup to V_{CCT_IO}	
PICD[1:0]	APIC Data	150 pullup to V_{CCT_IO}	Use a discrete resistor for each signal.
DPSLP#	Deep Sleep	1.5 kΩ pullup to V_{CCT_IO}	Not supported by 440MX
SMI#	System Management Interrupt	270 Ω pullup to V_{CCT_IO}	
STPCLK#	Stop Clock	680 Ω pullup to V_{CCT_IO}	

8.4.8. 440MX SDRAM Memory Interface Signals

1. See Section *6 – System Memory Design Guidelines* for more information.
2. All unused output memory signals should be left unconnected.
3. MD[63:0] should have series termination resistors. Resistor packs are recommended. See Section 6.2.1.
4. SDRAM control signals drive the memory array directly without any external buffers.
5. All the memory interface signals have a programmable buffer strength to optimize for different signal loading conditions.

8.4.9. 440MX PCI Bus Signals

1. The "south cluster" of 440MX is logically hard-wired to IDSEL 18 (device 7). Do not use this IDSEL for other PCI devices. As with the 440BX Chipset, the host-to-PCI bridge is hard-wired to IDSEL 11 (device 0). Even though 440MX does not support AGP, a design should probably avoid IDSEL 12 (device 1), which is typically the IDSEL for an AGP bridge.
2. All IDSEL signals for motherboard PCI devices should have a 100-Ω series resistor at each device.
3. 440MX's PCI interface is 5-V tolerant but drives at only 3 V. The following pullup recommendations assume the PCI bus is 3 V. Refer to Intel® 82443MX PCISet Electrical and Thermal Specification Datasheet Addendum and/or the PCI specification for pullup values for a 5-V PCI bus.
4. In a 3.3-V PCI environment, provide 10-kΩ pullups resistors to V3S on FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, and SERR# on the PCI bus.
5. 440MX does not implement the PERR# pin. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE).
6. The fourth PCI master REQ/GNT pair, PREQ[3]# and PGNT[3]#, are muxed with GPIO[29] and GPIO[30], respectively. If used as a PCI REQ/GNT pair, PREQ[3]# and PGNT[3]# should both have 10-kΩ pullup resistors to V3S.
7. PC/PCI REQ/GNT pair REQA#/GNTA# are muxed with GPIO[2] and GPIO[3], respectively. If used as a PC/PCI REQ/GNT pair, pull up both of these signals to V3S with 10-kΩ resistors.
8. PCI interrupt C and D channels are muxed with GPIO[22] and GPIO[23], respectively. If used as PIRQ[C]# and PIRQ[D]#, they must be pulled up.
9. Serial IRQ signal SERIRQ is muxed with GPIO7. Pull up to V3S with a 10-kΩ resistor if used as SERIRQ.
10. CLKRUN#: An (8.2 k-10 kΩ) pullup to V3S should be placed on the CLKRUN# signal.

Table 13. 440MX PCI Bus Signals

Signal	Termination Resistor	Pullup or Pulldown Resistor
AD[31:0]	None	None
C/BE[3:0]#	None	None
FRAME#	None	10 kΩ pullup to V3S
DEVSEL#	None	10 kΩ pullup to V3S
IRDY#	None	10 kΩ pullup to V3S
TRDY#	None	10 kΩ pullup to V3S
STOP#	None	10 kΩ pullup to V3S
LOCK#	None	10 kΩ pullup to V3S
REQ[2:0]#	None	10 kΩ pullup to V3S
GNT[2:0]#	None	10 kΩ pullup to V3S if used
REQ3#/GNT3#	None	10 kΩ pullup to V3S if used as PCI REQ / GNT (signals muxed with GPIO[29,30])
PAR	None	None
SERR#	None	10 kΩ pullup to V3S
CLKRUN#	None	8.2 k – 10 kΩ pullup to V3S
PCIRST#	None	None
REQA/GNTA	None	10 kΩ pullup to V3S if used as REQA/GNTA (signals muxed with GPIO[2,3])
PIRQ[B:A]#	None	10 kΩ pullup to V3S
PIRQ[D:C]#	None	10 kΩ pullup to V3S if used as PCI interrupts (signals muxed with GPIO[22,23])
SERIRQ	None	10 kΩ pullup to V3S if used as SERIRQ (signal muxed with GPIO[7])

8.4.10. 440MX IDE Interface

1. 470-Ω pulldown resistor on pin 28 of the IDE connectors (CSEL). Support of Cable Select (CSEL) is a PC97 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
2. Primary IDE channel (the only channel supported by 440MX) uses IRQ14.
3. All signals running to IDE connectors must have series terminating resistors (33Ω). These series termination resistors should be placed as close as possible to 440MX. If the distance between 440MX and the connector is greater then 4 inches, the terminating resistor should be placed within 1 inch of 440MX.
4. Series resistors may or may not be necessary on PIORDY. A system designer should perform simulations in order to determine if series resistors are required.
5. If using ISA reset signal RSTDRV from 440MX, it should be routed through a Schmitt trigger for RESET# signals to the IDE channel.
6. Ground pins 2, 19, 22, 24, 26, 30 and 40 of ATA connectors.
7. No connect pins 20 of the ATA connector.

8. Pin 34 of the ATA connector is PDIAG for IDE interface; if multiple IDE connectors are used, connect each pin 34 together. If a single IDE connector is used, pin 34 can be left unconnected.
9. According to ATA-4 spec, a 10-kΩ pulldown resistor is required on PD7 to allow a host to recognize the absence of a device at power-up.

Table 14. 440MX IDE Signals

Name	Termination Resistor	Pullup or Pulldown Resistor
PDCS1#	33 Ω	None
PDCS3#	33 Ω	None
PDA[2:0]	33 Ω	None
PDD[15:0]	33 Ω	10 kΩ pulldown resistor on PDD[7] only.
PDDACK#	33 Ω	None
PDDRQ	33 Ω	5.6 kΩ pulldown resistor
PDIOR#	33 Ω	None
PDIOW#	33 Ω	None
PIORDY	33 Ω (may not need)	1 kΩ pullup resistor to V3S
CSEL (does not connect to 440MX)	None	470 Ω pulldown resistor

8.4.11. USB Interface

1. Refer to the "*PIIX4 USB Design Guide*" for the layout recommendations for USB, clock, over current detection circuit and general board layout recommendations.

8.4.12. AC'97 Interface

1. If the AC'97 interface is not used, leave unconnected. Internal pullup and pulldown resistors will ensure the unused AC'97 interface is not floating.

8.4.13. 440MX X-bus Signals

1. 440MX implements a 5V-tolerant, 3V-drive X-bus interface. During POS, many X-bus signals are actively driven by the chipset. For this reason, if a design implements POS, X-bus signals should be pulled up to V3S to avoid unnecessary leakage. If POS is not supported, V5S is acceptable.
2. GPIO[6] / IRQ8# defaults to a GPIO; the IRQ8# function is in the resume well, but the GPIO[6] function is in the core well (see Section 8.4.15 for details). If used as IRQ8#, an external 10 kΩ pullup to V3RSM is required. If used as GPIO[6], an external pullup to V3 may be required to ensure a valid logic level.
3. DMA channel 3 signals, DREQ3 and DACK3#, are muxed with GPIO[27] and GPIO[28], respectively. If the DMA channel is used, pull DREQ3 down with a 4.7-kΩ resistor.
4. The 440MX does not support an address enable signal AEN; instead, the chipset drives 0x00000 on the X-Bus address bus for DMA transactions, and there is no danger of address confusion. Tie AEN inactive low to devices that have AEN inputs. Alternatively, AEN can be generated externally using glue logic on the board to drive AEN when a DMA acknowledge signal is asserted.
5. ZEROWS# is muxed with GPIO[21]. If used as ZEROWS#, pull up with a 1-kΩ resistor to V3S.

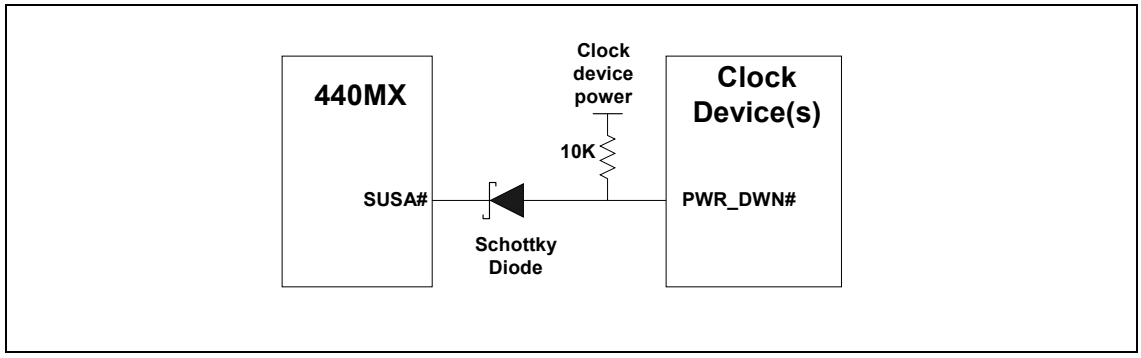
Table 15. 440MX X-bus Signals

Name	Termination Resistor	Pullup or Pulldown Resistor
IOCHRDY	None	1 kΩ pullup resistor to V3S
IOR# / IOW# / MEMR# / MEMW#	None	4.7 kΩ pullup resistors to V3S
RSTDRV	None	Pullup
SA[18:0]	None	None
SD[7:0]	None	4.7 kΩ pullup resistors to V3S
SYSCLK	None	None
ZEROWS#	None	1 kΩ pullup resistor to V3S if used as ZEROWS# (signal is muxed with GPIO[21])
DRQ[2:0]	None	4.7 kΩ pulldown resistors.
DACK[2:0]#	None	None
DRQ3	None	4.7 kΩ pulldown resistor if used as DRQ3 (signal is muxed with GPIO[27])
DACK3#	None	None if used as DACK[3]# (signal is muxed with GPIO[28])
TC	None	None
IRQ[14,12,7:3,1]	None	10 kΩ pullup resistor to V3S

8.4.14. Power Management Signals

1. Power management signals that reside in the suspend well requiring pullup resistors must be pulled up to V3RSM. Note that these signals do not support 5-V input levels.
2. EXTSMI# is an input at reset and an open drain output if activating an SMI# within the Serial IRQ function. Designers may need an 8.2-kΩ pullup to V3RSM if it is not always being driven to a valid state.
3. CLKRUN# requires a (8.2 k –10 kΩ) pullup to V3S.
4. PCI_STP# should be connected to the clock synthesizer to stop the PCI clocks.
5. CPU_STP# should be connected to the clock synthesizer to stop the CPU clock.
6. SUSA# is connected to the clock synthesizer's PWR_DWN# pin through a Schottky diode with a 10-kΩ pullup. Alternatively, SUSA# may be used to control the clock synthesizer's power plane.

Figure 21. SUSA# Connected to PWR_DWN# of Clock Synthesizer



7. SUSB#, SUSC# can be connected to control the power planes.
8. THERM# should be connected to the thermal protection logic.
9. RI# should be connected to the modem if this feature is used.
10. BATLOW# should be connected to the battery monitoring logic if the feature is implemented.
11. LID is connected to the lid monitoring logic of the system.
12. PWRBTN# should be connected to logic that allows the user to switch to and from suspend.
13. RSMRST# should be connected to switch to allow a complete system reset. Note that this signal resides in the V_{CC}(RTC) well; hence its potential must not exceed that of V_{CC}(RTC).
14. SMBCLK and SMBDATA can be used as SMBus signals or I^2C signals. When used in an SMBus environment, there are restrictions on the maximum capacitance and pullup current on these signals. Refer to the *System Management Bus Specification.*

8.4.15. General Purpose I/O Signals

The following are the rules that govern the functionality of 440MX's GPIOs:

1. GPIOs that are MUXed with functions default to the functional use EXCEPT for GPIOs that have the same alternate function as in PIIX4E (REQA#, GNTA#, SERIRQ, and IRQ8#), in which case they follow the PIIX4E programming model.
2. Some GPIOs are powered by the resume well (see #3 below). The core well powers the rest well. GPIOs that are powered by the resume well can be programmed to retain their programming during STR and STD / SOFF (these GPIOs are reset by the assertion of RSMRST# and not PCIRST#) – i.e., inputs can be used to wake the system, and outputs can be programmed to retain their state. GPIOs that are powered by the core well will be tri-stated during STR and are not powered during STD / SOFF.
3. GPIOs that default to functions powered by the resume well are only powered by the resume well when used as that default function. If used as a GPIO, those pins do not behave as if powered by the resume well (i.e., they do not retain their programming through STR and STD / SOFF).
4. GPIOs that default to GPIOs (not functional signals), default to inputs.
5. GPIOs [0, 4, 9, 17, 18, 20] are capable of generating SCI and SMI like GPIO[1]. These GPIOs can also generate resume events.
6. All unused GPIO signals should be pulled to a valid logic level with 10-kΩ resistors. If pulled high, they should be pulled to V3S except for the GPIOs that are in the resume well, which should be pulled to V3RSM.
7. All unused outputs can be left as no-connects.

Consider the default functional use of GPIOs when assigning active low and active high outputs to these pins. Note the power wells that supply the GPIOs and also consider this for assigning GPIOs that need to stay active through suspend. As noted above, GPIOs powered by the resume well can retain their values during STR and also STD / SOFF.